FIG. 1

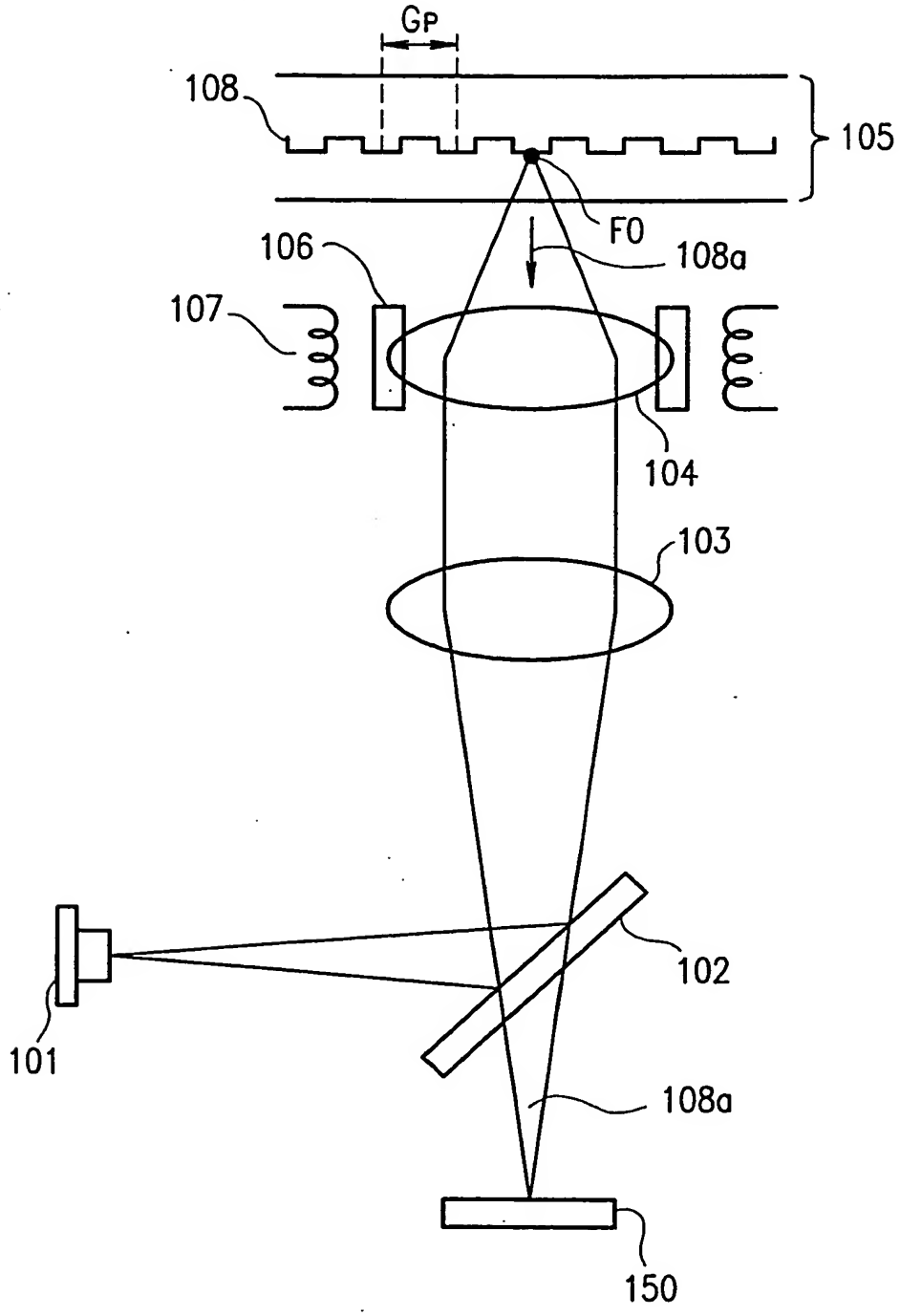


FIG. 2

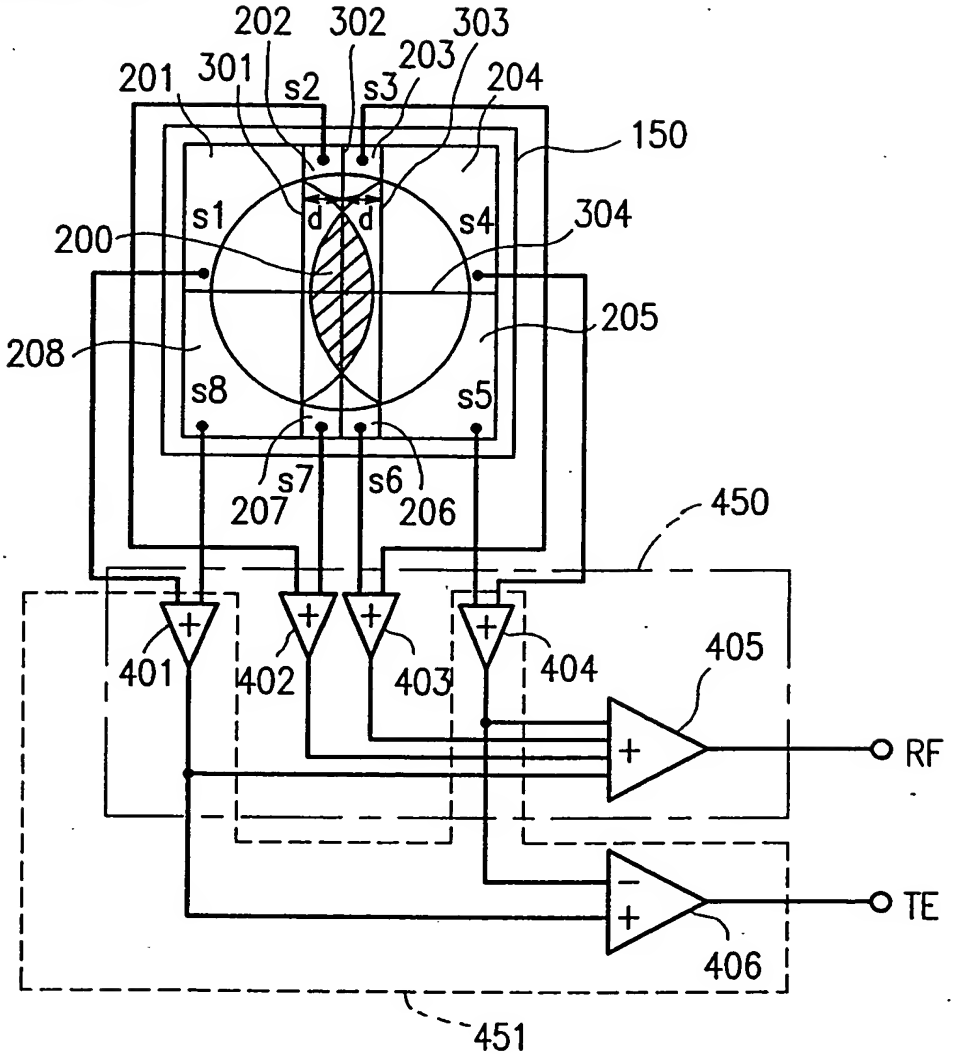

202
302
303
201
301
s2
s3
203
204
150
s1
d
d
s4
304
200
205
208
s8
s5
s7
s6
207
206
450
401
402
403
404
405
RF
TE
406
451

FIG. 3

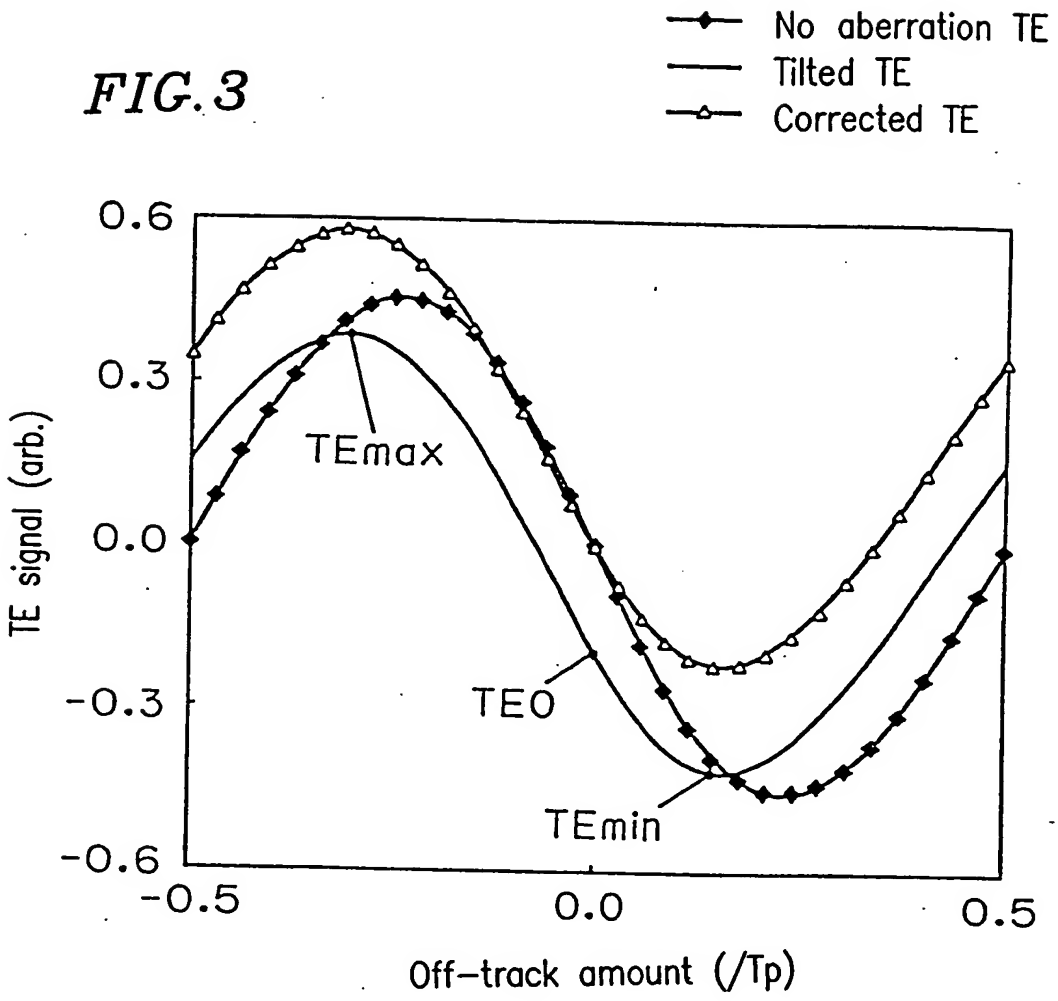

No aberration TE
Tilted TE
Corrected TE
0.6
0.3
0.0
-0.3
-0.6
TE signal (arb.)
TEmax
TEO
TEmin
-0.5
0.0
0.5
Off-track amount (/Tp)

FIG. 4

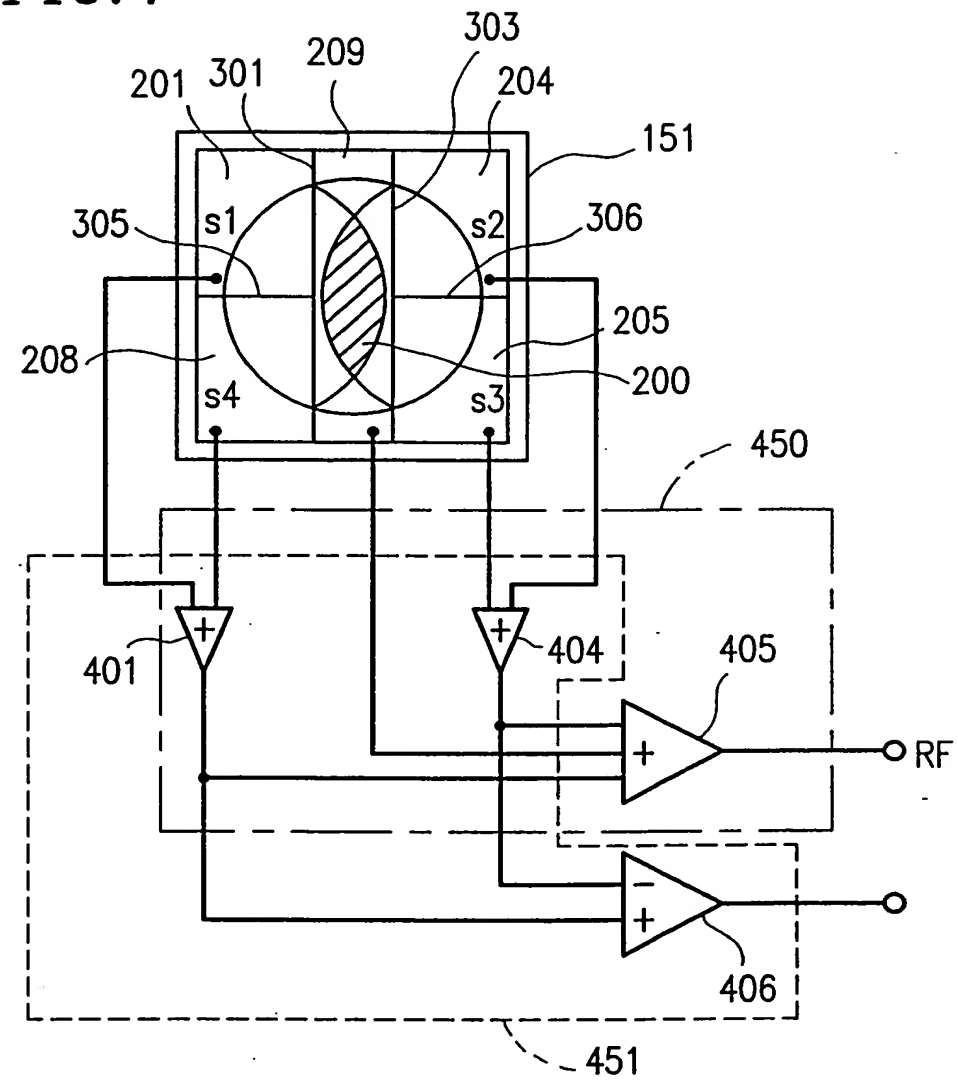

303
209
201
301
204
151
305
s1
s2
306
205
208
200
s4
s3
450
401
404
405
RF
406
451

FIG. 5

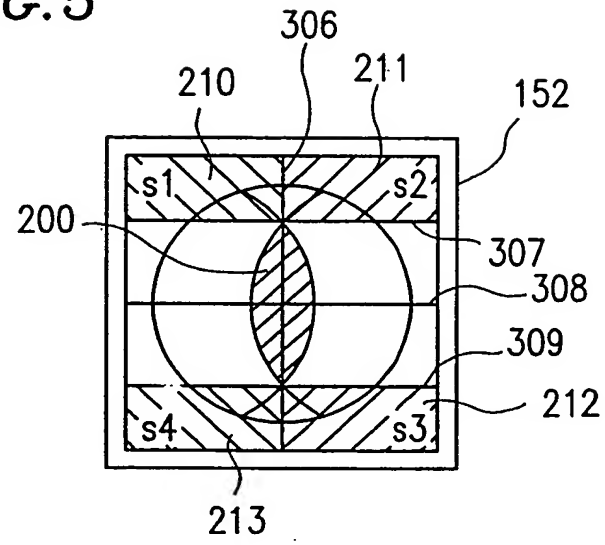

306
210
211
152
s1
s2
200
307
308
309
212
s4
s3
213

FIG. 6

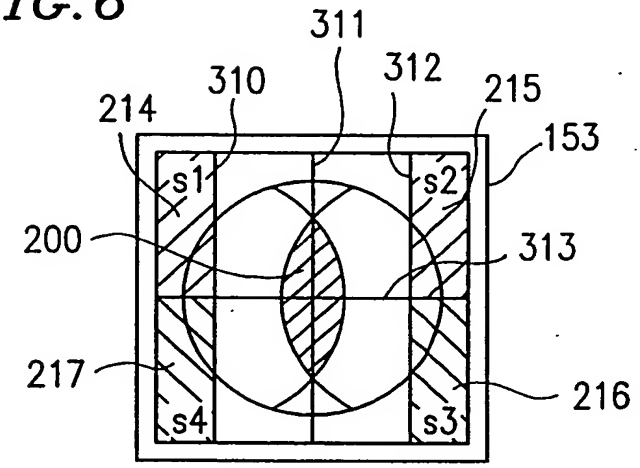

311
310
312
215
214
153
s1
s2
200
313
217
216
s4
s3

FIG. 7

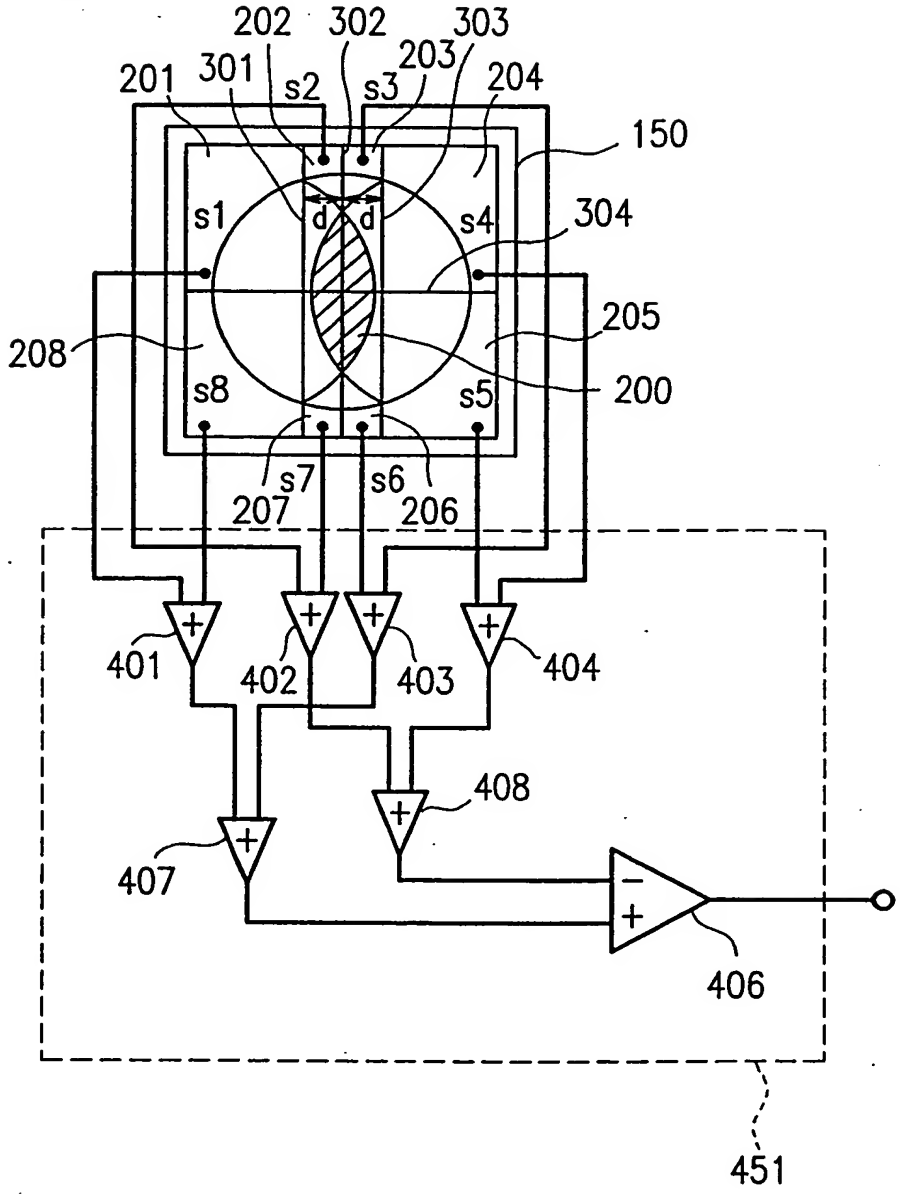

202
302
303
201
301
s2
s3
203
204
150
s1
d
d
s4
304
205
208
200
s8
s5
s7
s6
207
206
401
402
403
404
408
407
406
451

FIG. 8

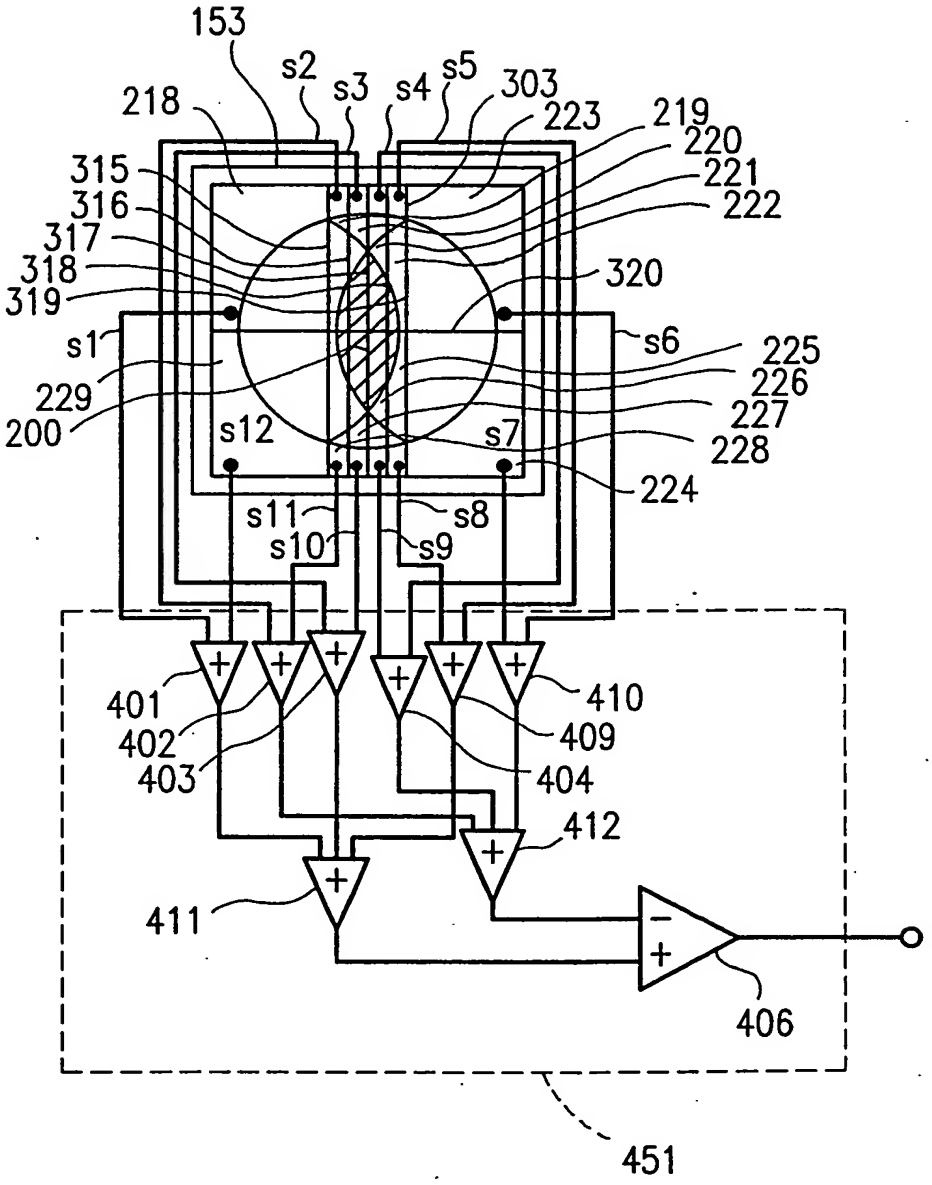

153
s2
s3
s4
s5
303
218
223
219
220
221
222
315
316
317
318
319
320
s1
s6
225
226
227
228
229
200
s12
s7
224
s11
s8
s10
s9
401
402
403
410
409
404
412
411
406
451

FIG. 9

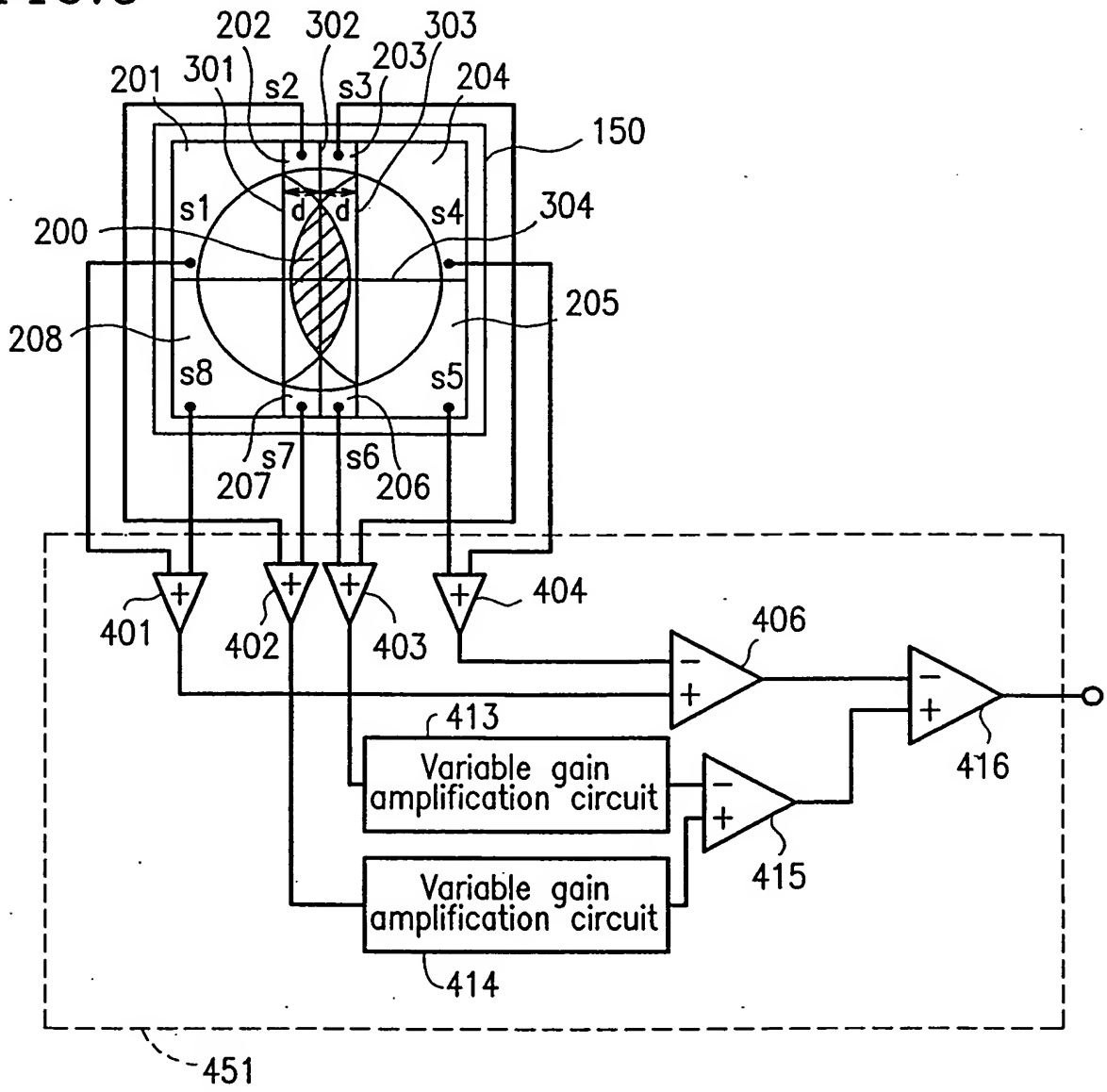

202
302
303
201
301
s2
s3
203
204
150
s1
d
d
s4
304
200
205
208
s8
s5
s7
s6
207
206
401
402
403
404
406
413
Variable gain amplification circuit
Variable gain amplification circuit
415
416
414
451

FIG. 10A

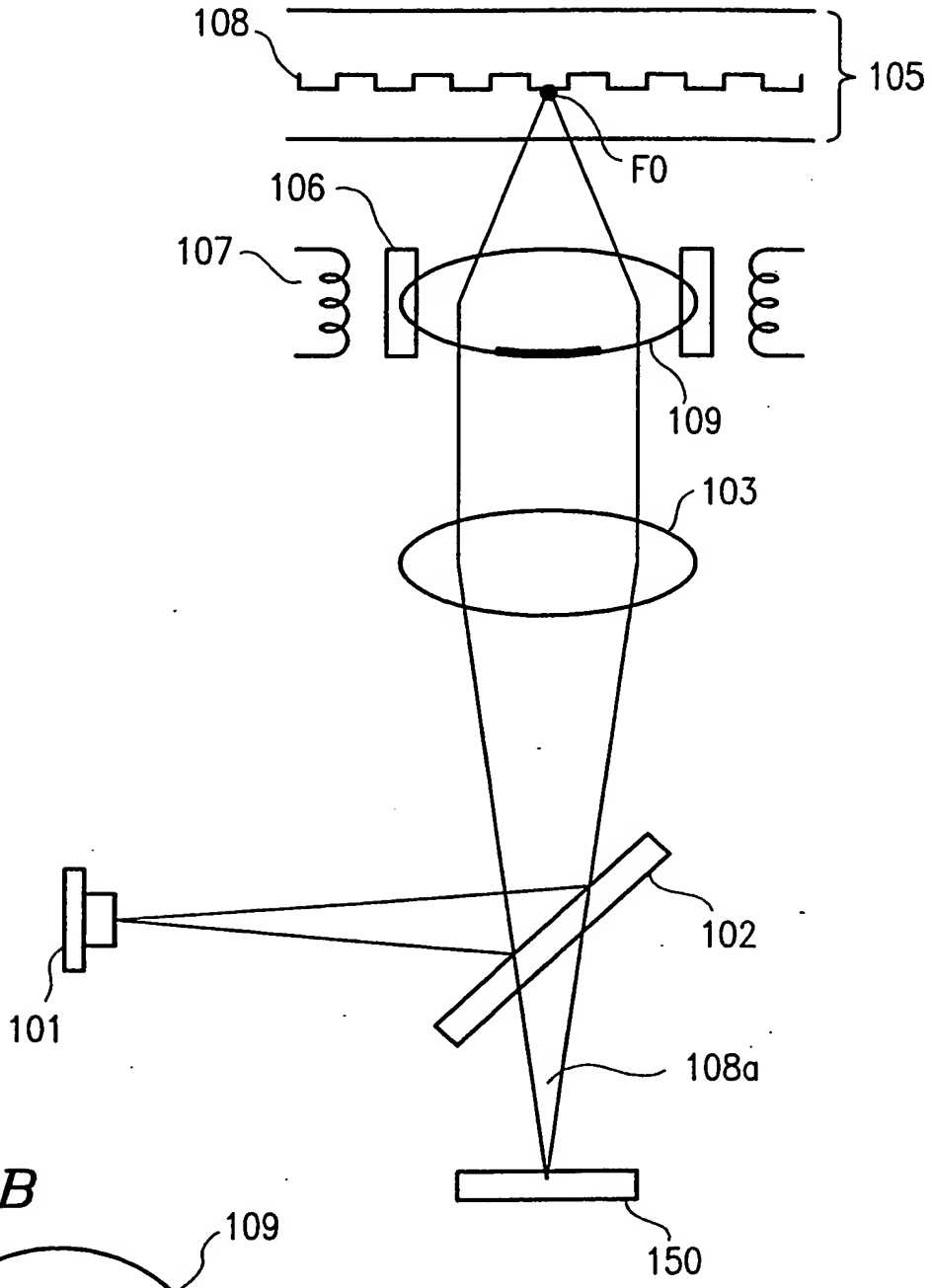


FIG. 10B

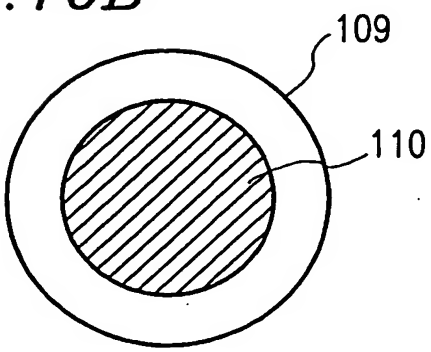


FIG. 11

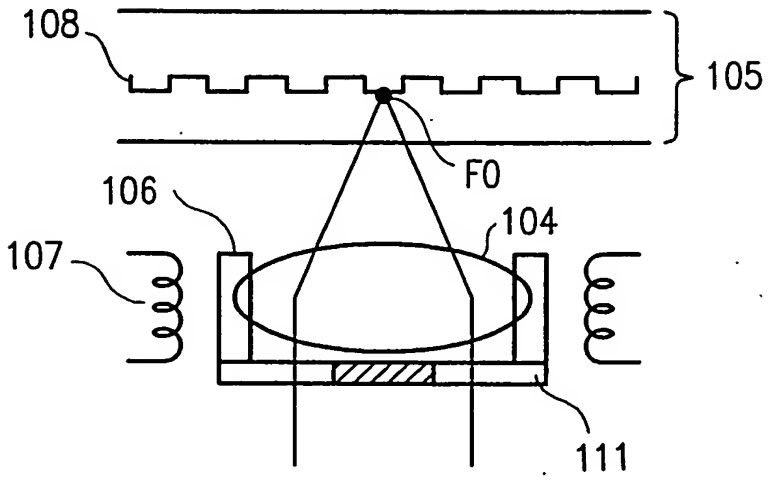


FIG. 12

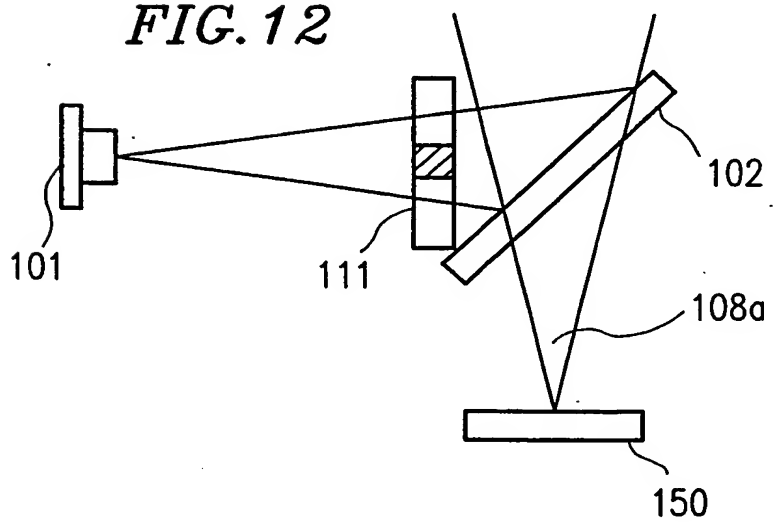


FIG. 13

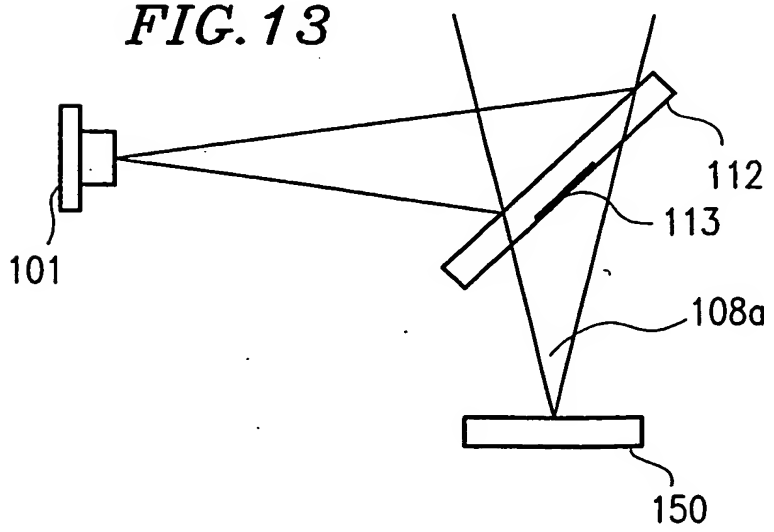


FIG. 14

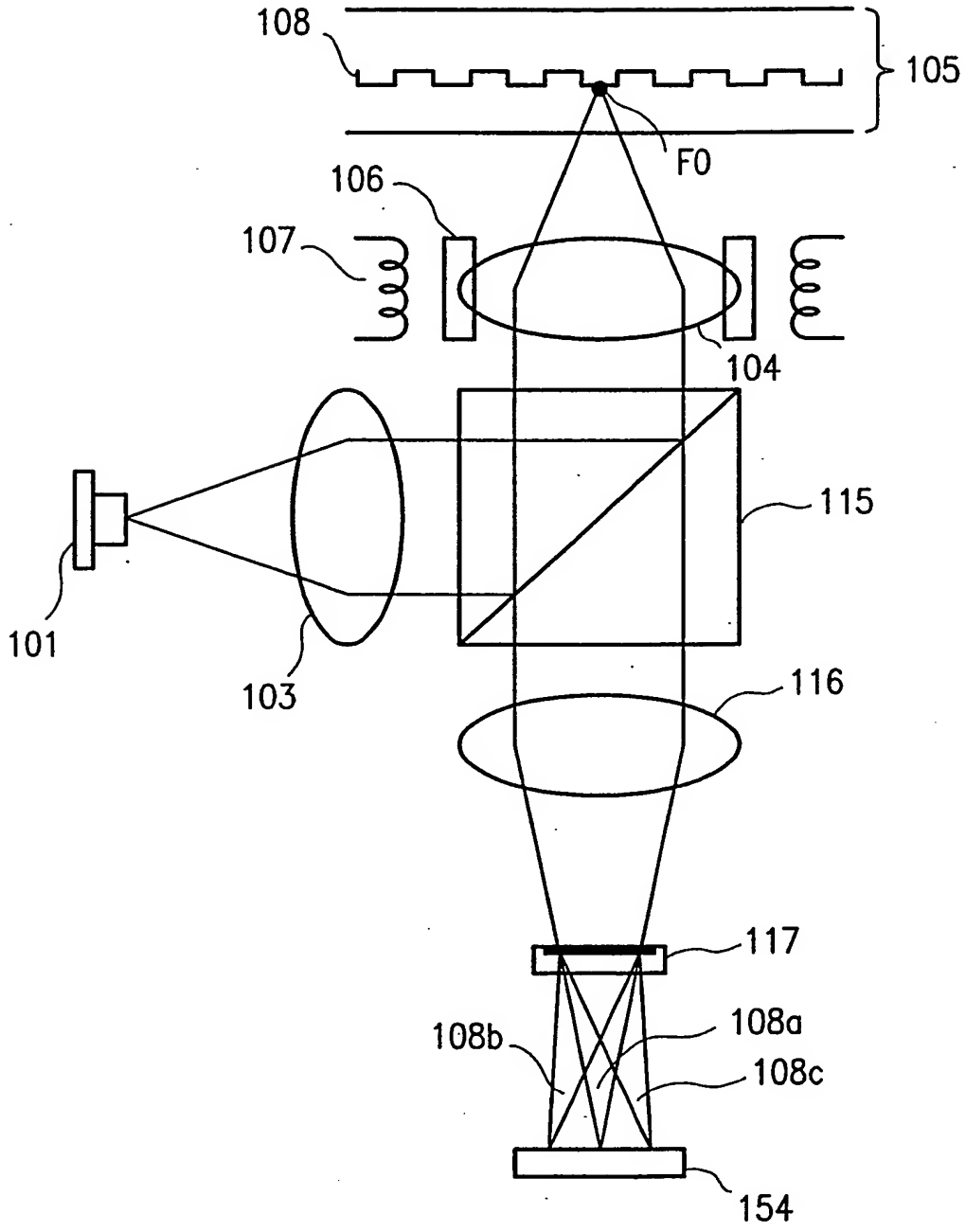


FIG. 15

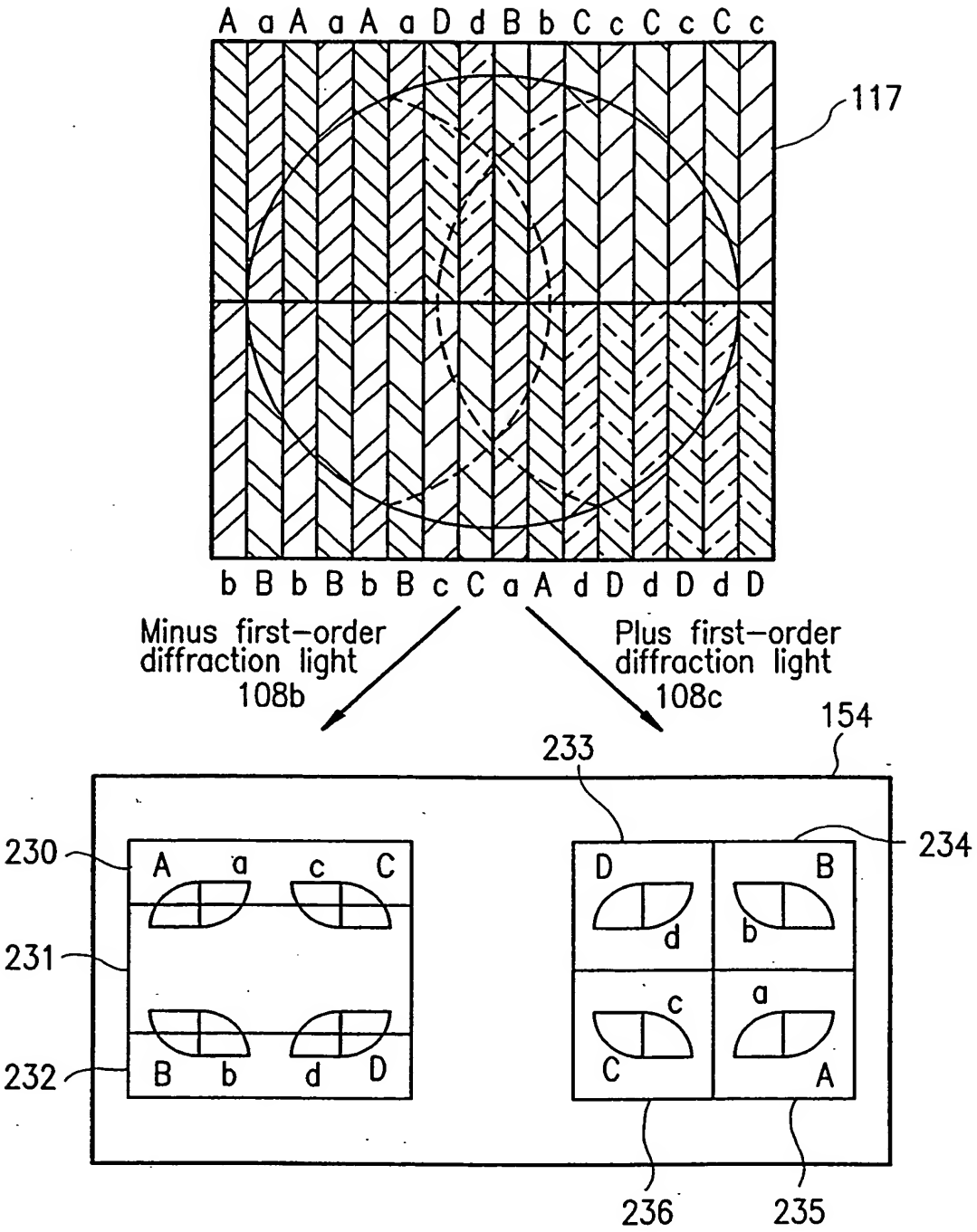

A a A a A a D d B b C c C c C c
117
b B b B b B c C a A d D d D d D
Minus first-order diffraction light
108b
Plus first-order diffraction light
108c
154
233
230
231
232
234
A a c C
B b d D
D d
B b
C c
a A
236
235

FIG. 16

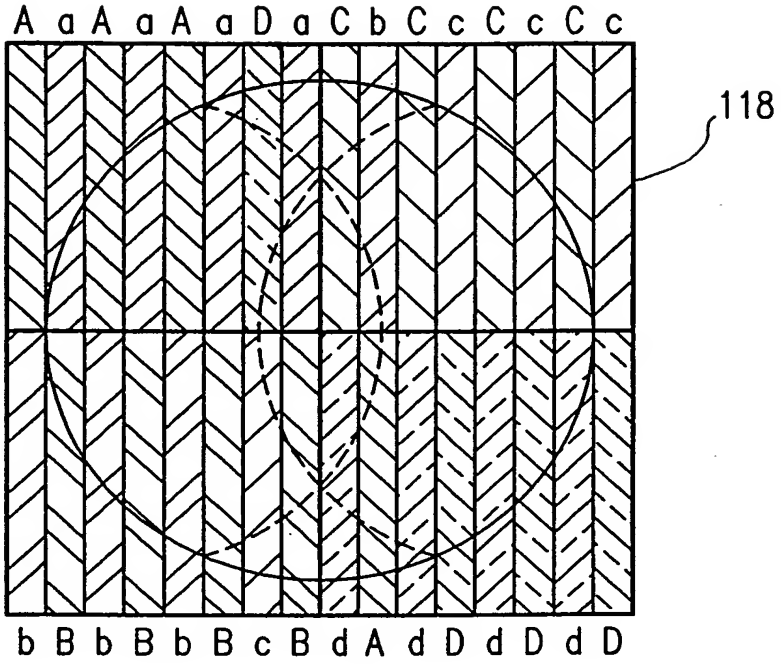


FIG. 17

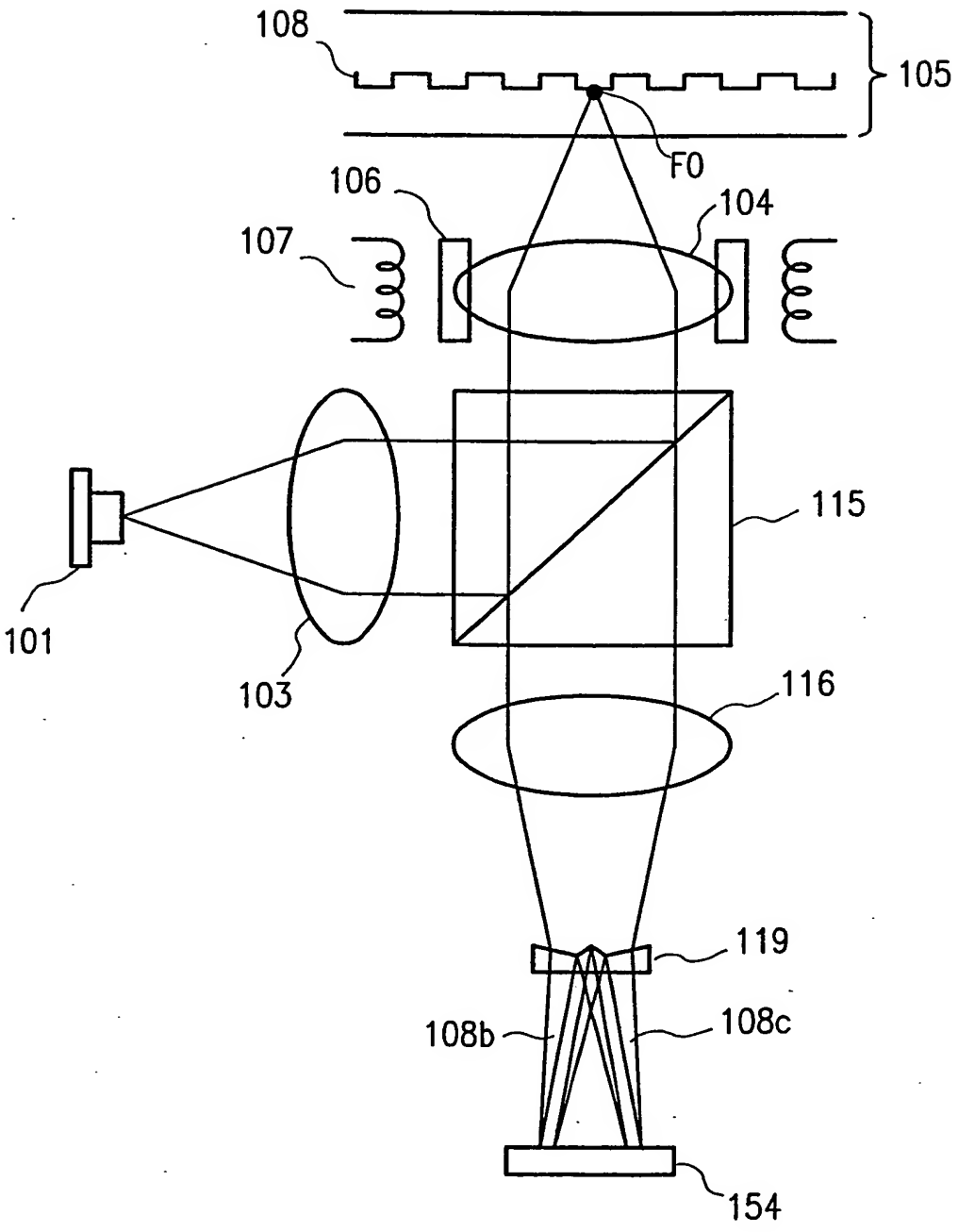


FIG. 18

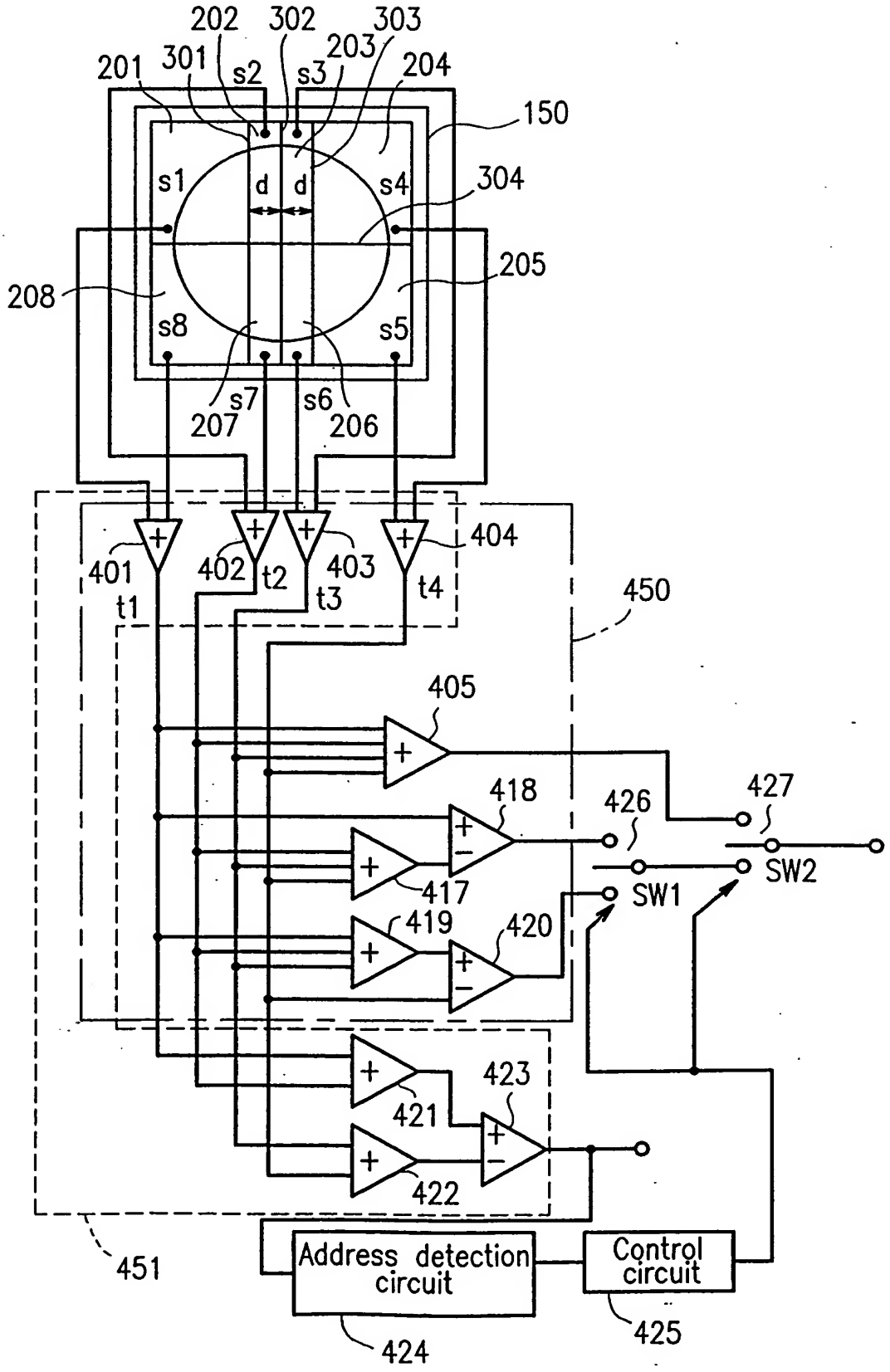

202
302
303
201
301
s2
s3
203
204
150
s1
d
d
s4
304
205
208
s8
s5
s7
s6
207
206
401
402
403
404
t1
t2
t3
t4
450
405
418
426
427
417
SW1
SW2
419
420
421
423
422
451
Address detection circuit
Control circuit
424
425

FIG. 19A

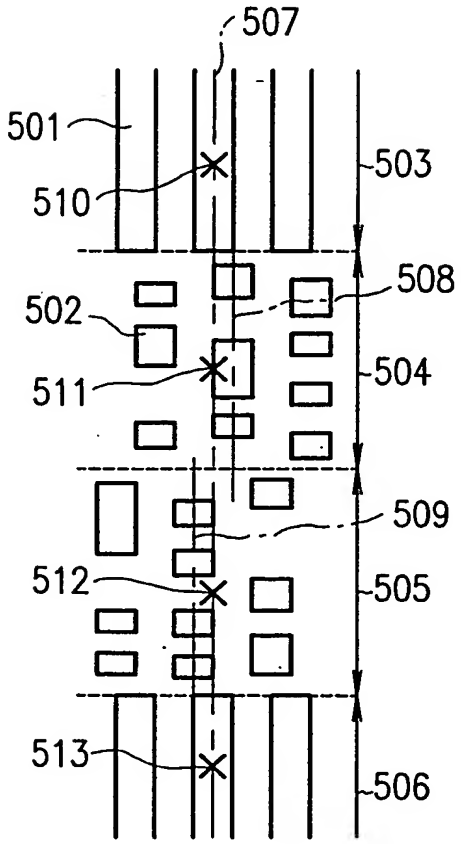


FIG. 19B

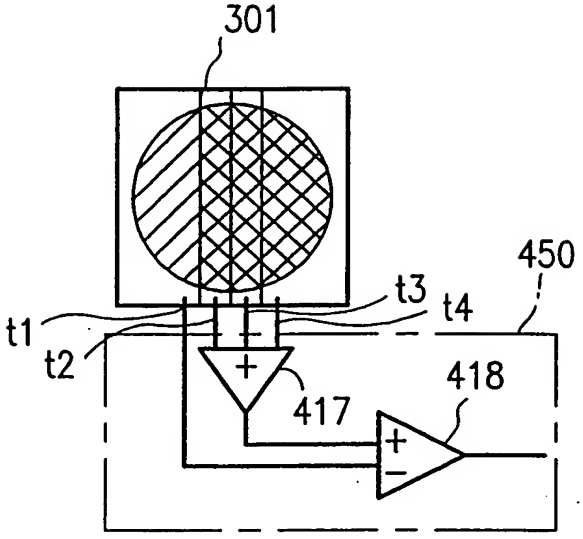


FIG. 19C

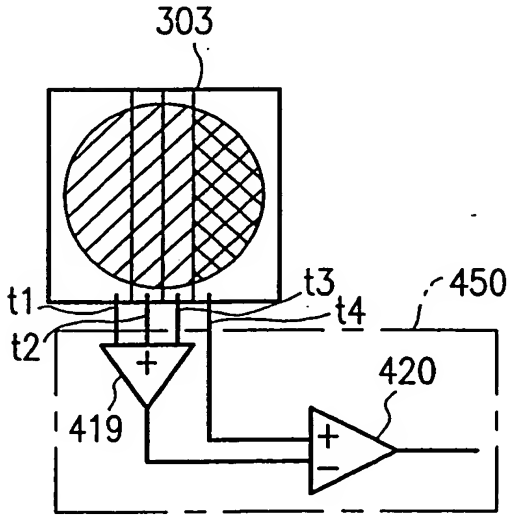


FIG. 20

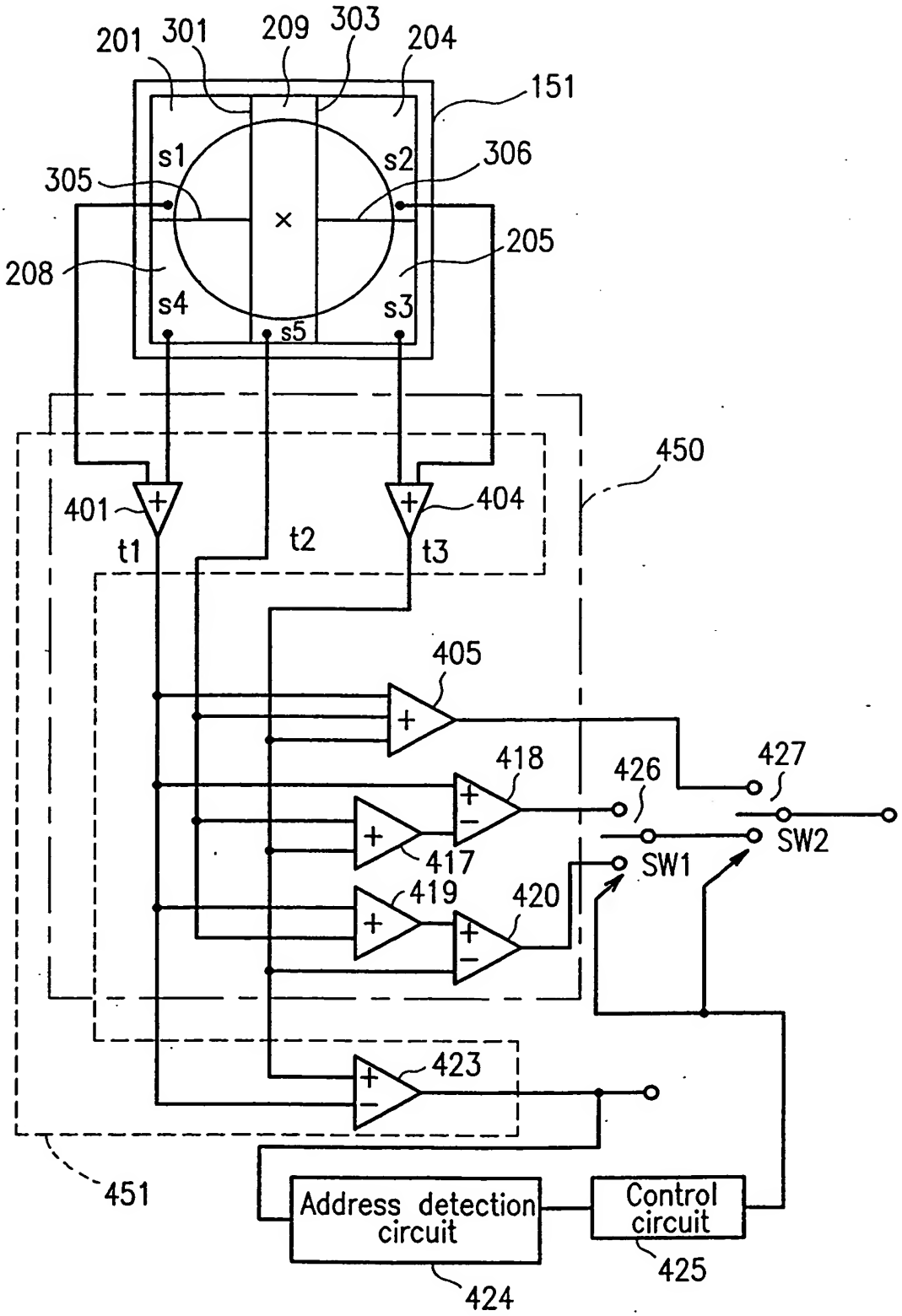

201
301
209
303
204
151
s1
s2
306
305
205
208
s4
s3
s5
450
401
404
t1
t2
t3
405
418
426
427
SW1
SW2
417
419
420
423
451
Address detection circuit
Control circuit
424
425

FIG. 21A

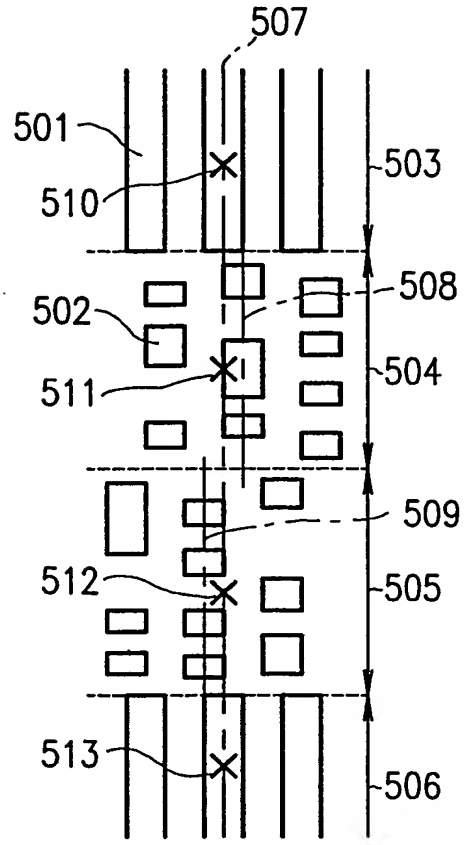


FIG. 21B

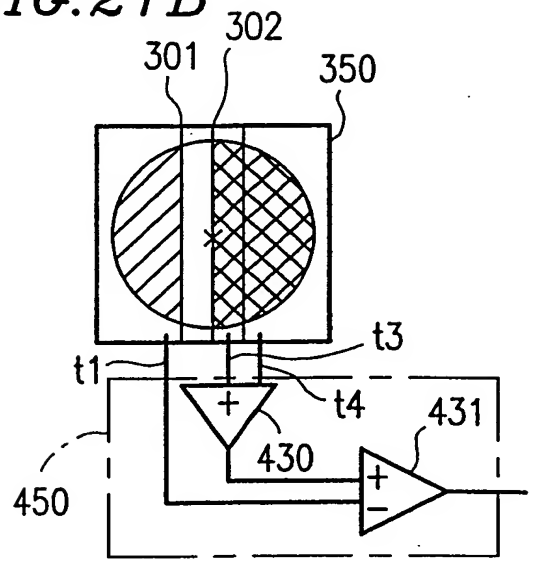


FIG. 21C

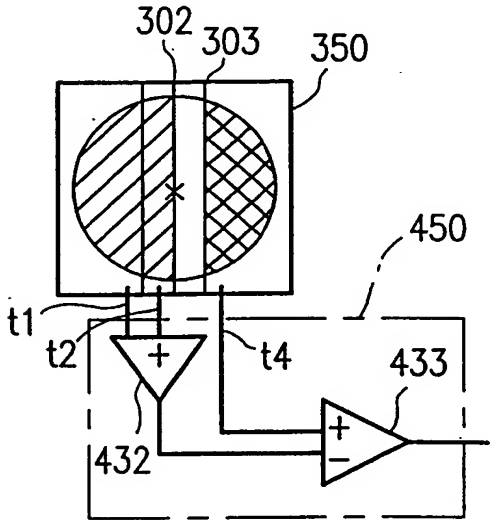


FIG. 22A

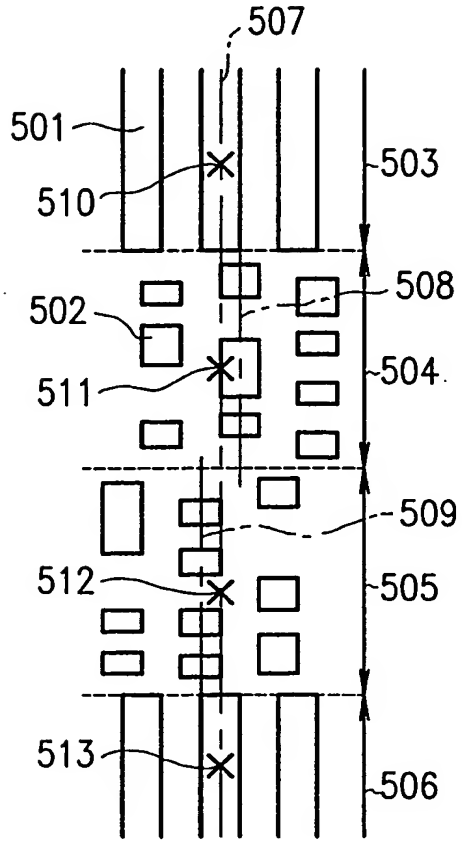


FIG. 22B

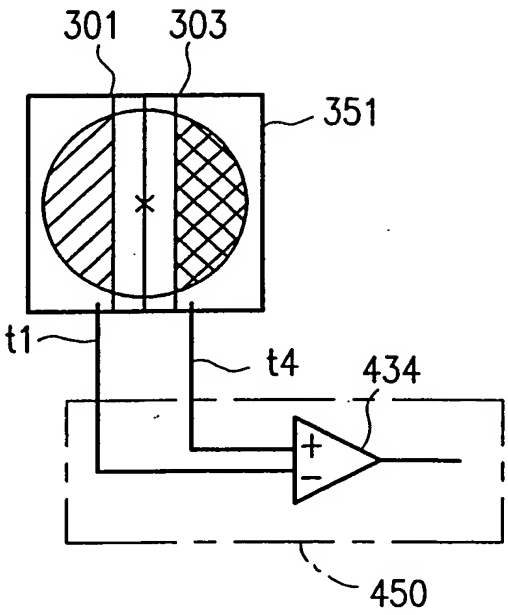


FIG. 23A

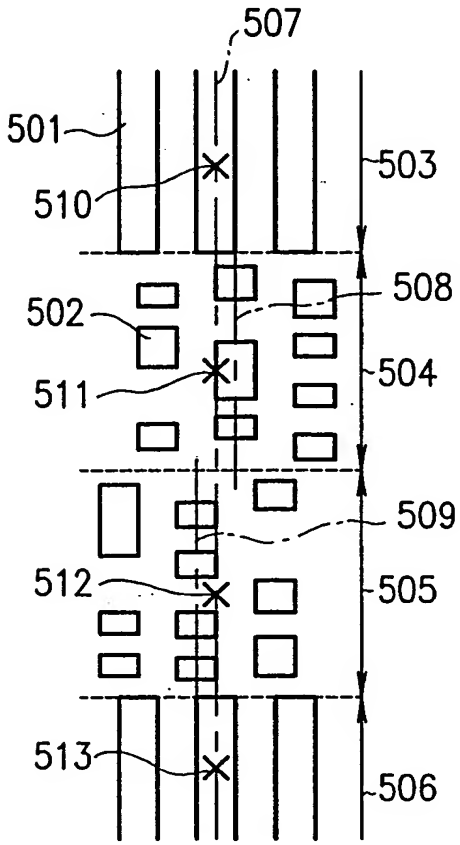


FIG. 23B

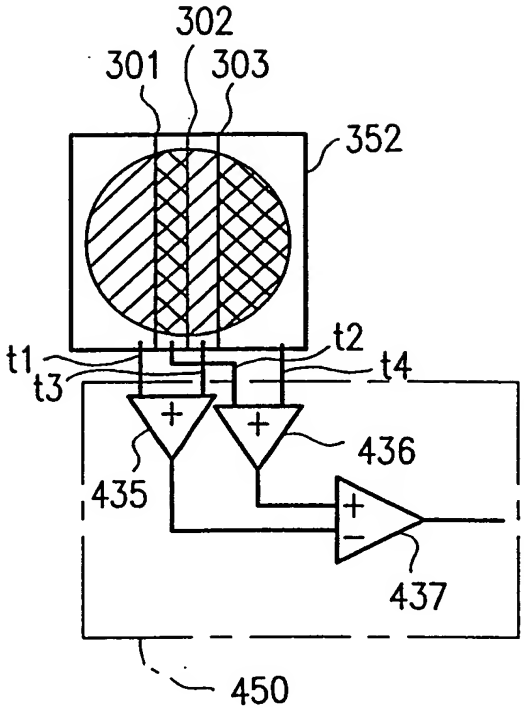


FIG. 24

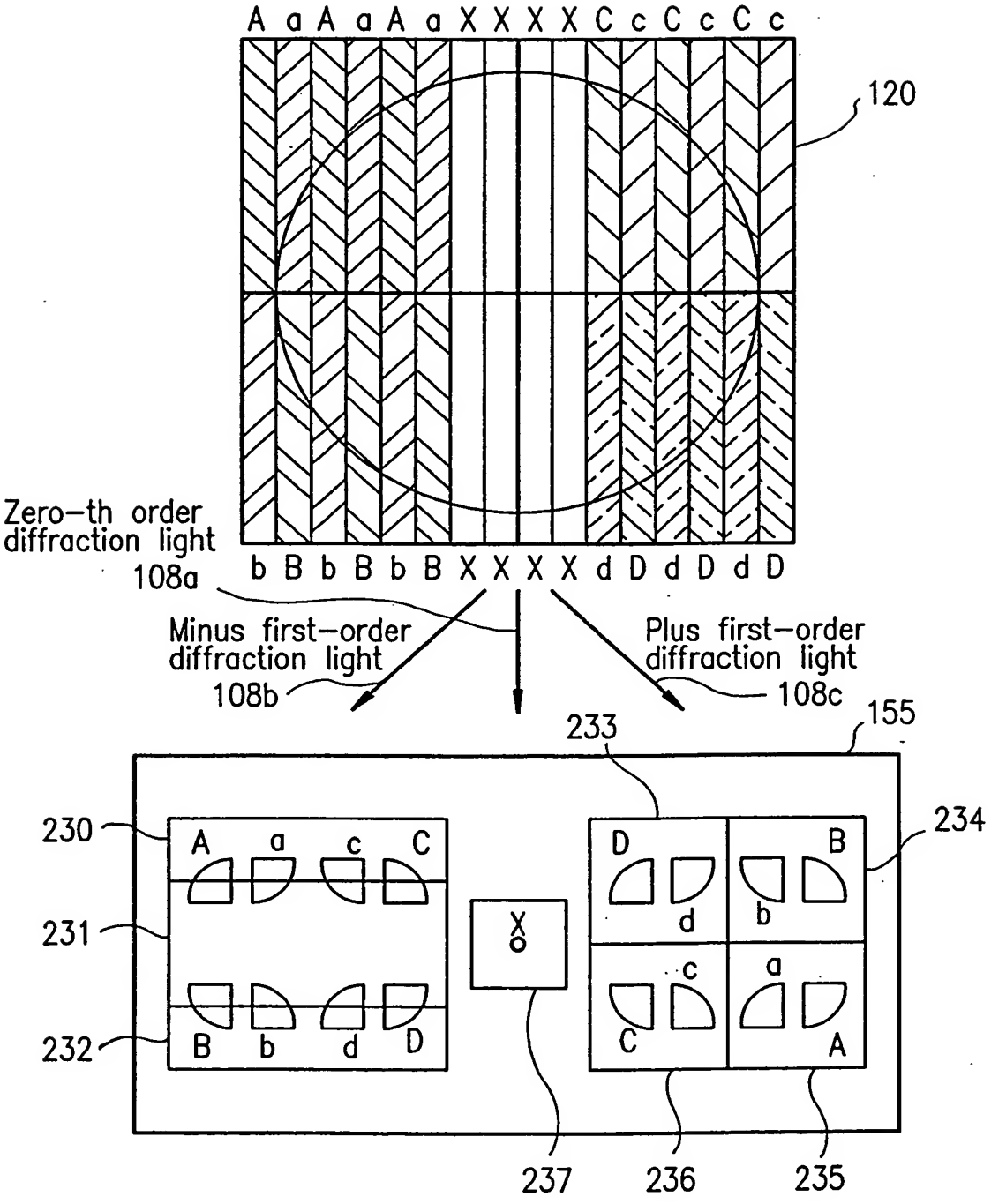

A a A a A a X X X X C c C c C c
120
Zero-th order diffraction light
108a
b B b B b B X X X X d D d D d D
Minus first-order diffraction light
108b
Plus first-order diffraction light
108c
155
233
230
231
232
234
A a c C
B b d D
X
O
D d
B b
c C
a A
237
236
235

FIG. 25

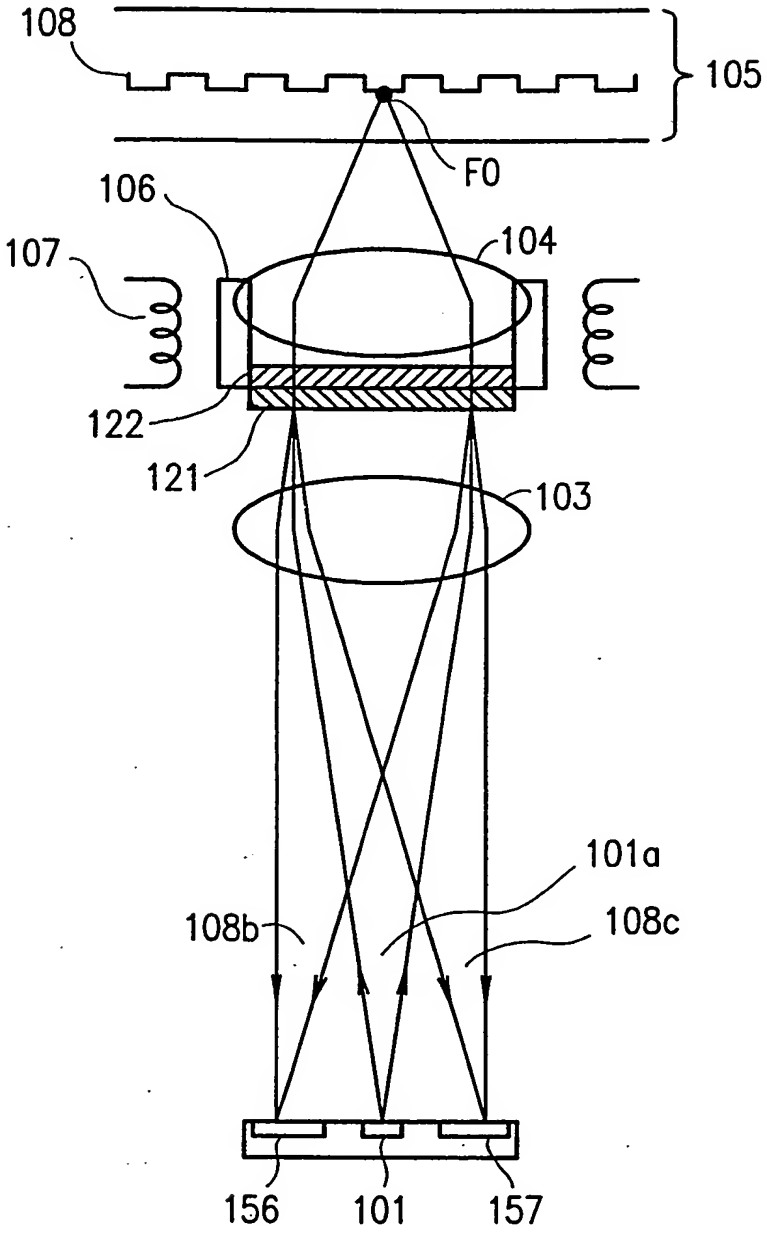


FIG. 26

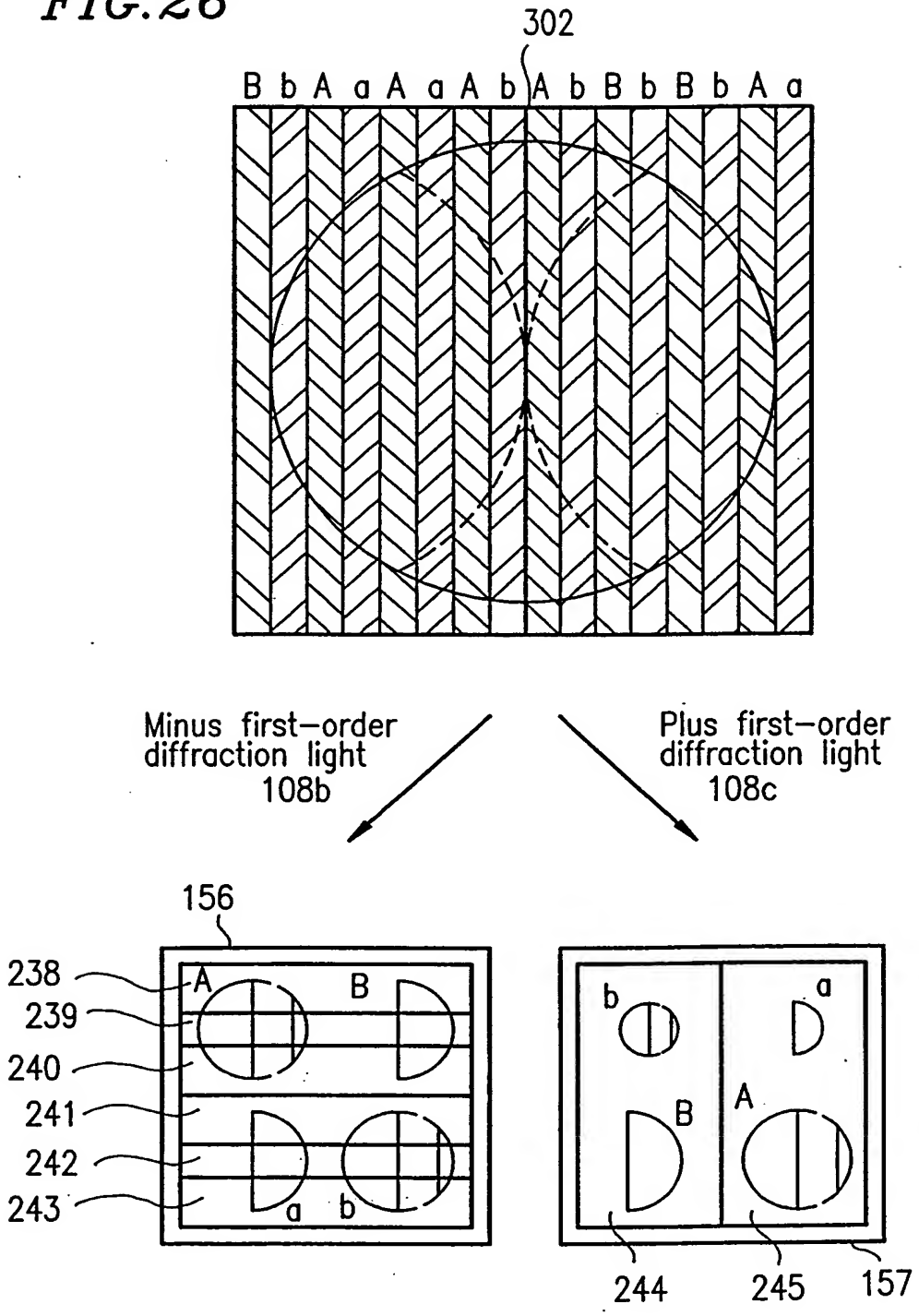

302
B b A a A a A b A b B b B b A a
Minus first-order diffraction light 108b
Plus first-order diffraction light 108c
156
238
239
240
241
242
243
A
B
a
b
b
a
B
A
244
245
157

FIG. 27

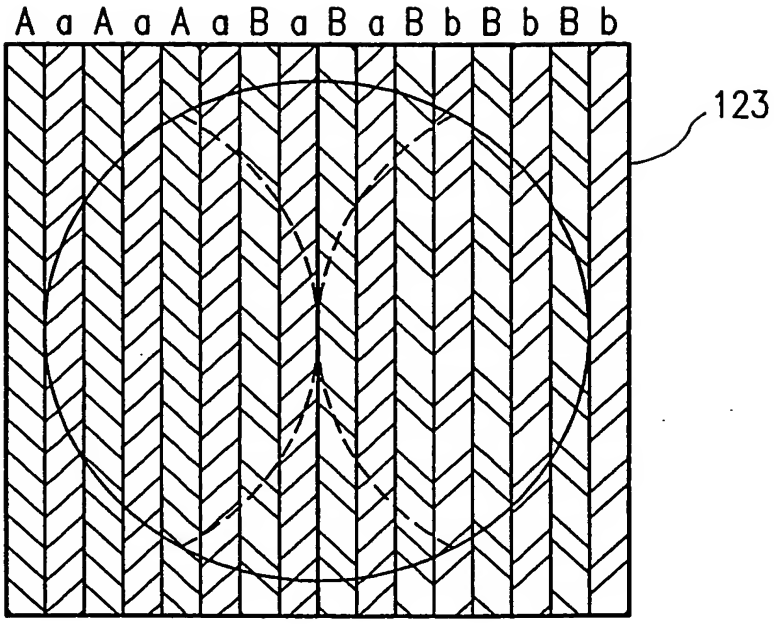
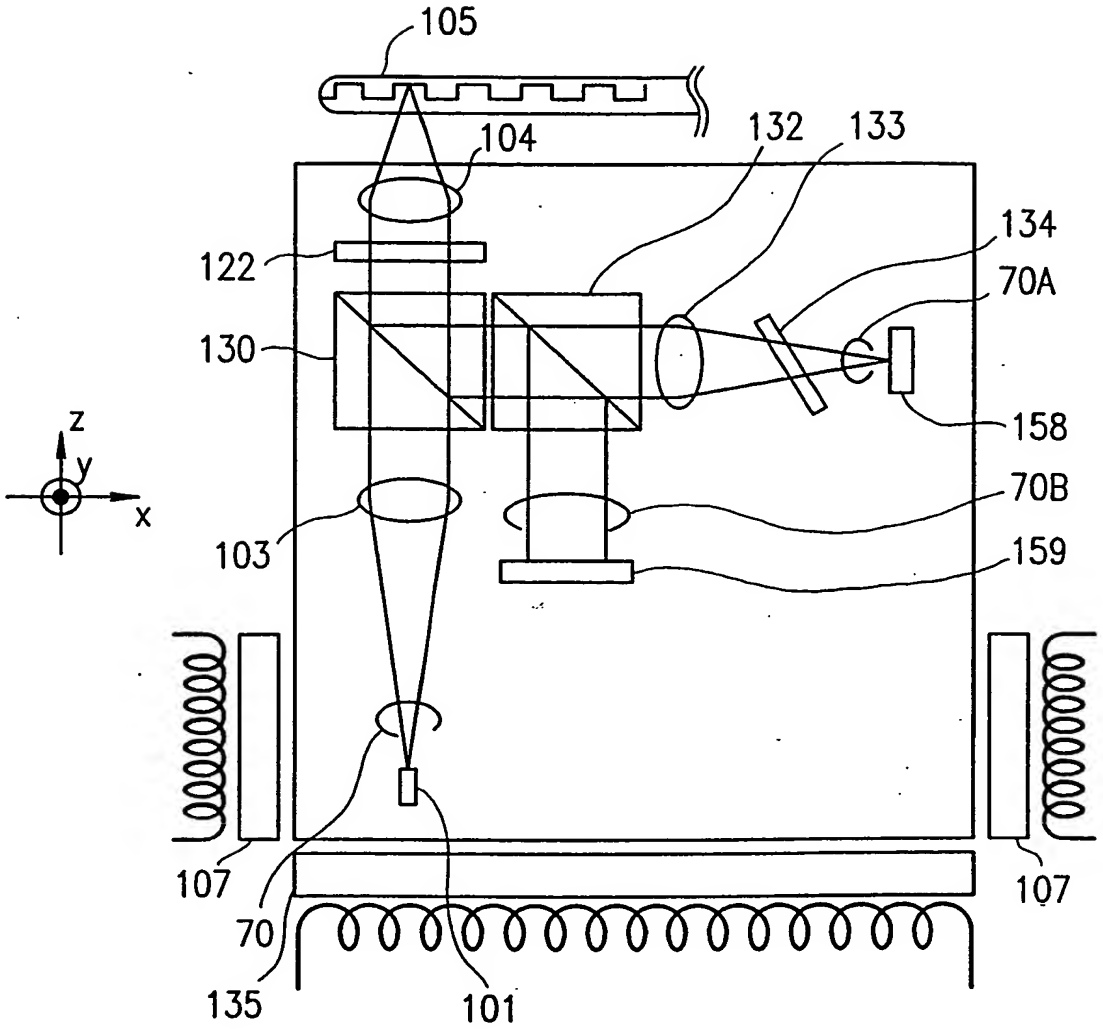


FIG. 28


105
104
132
133
134
122
70A
130
158
z
y
x
70B
103
159
107
107
70
135
101

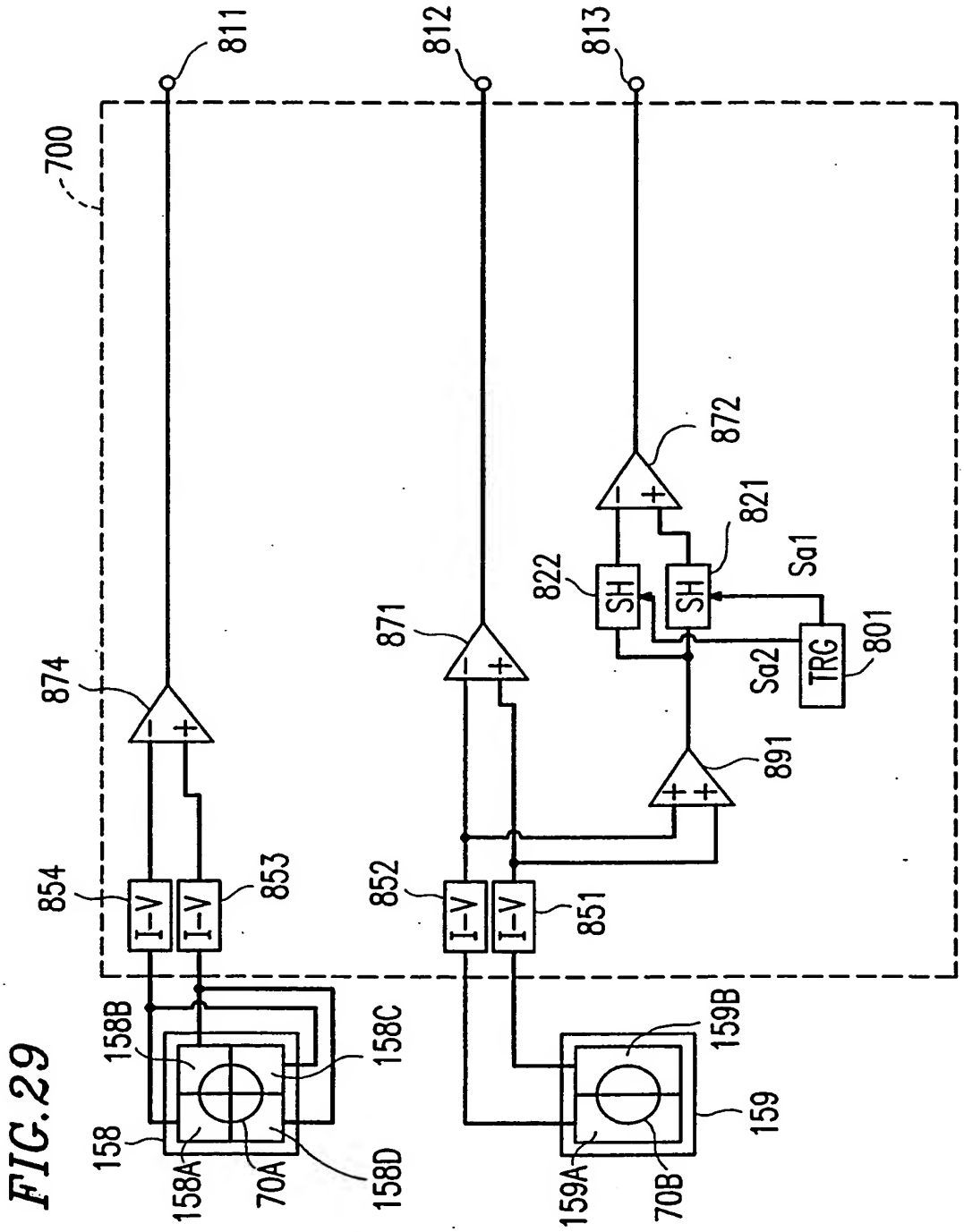

700
811
812
813
872
821
822
SH
SH
Sa1
871
801
TRG
Sa2
874
891
854
I-V
I-V
853
852
I-V
I-V
851
158B
158C
159B
158
159
158A
70A
158D
159A
70B

FIG.29

FIG. 30

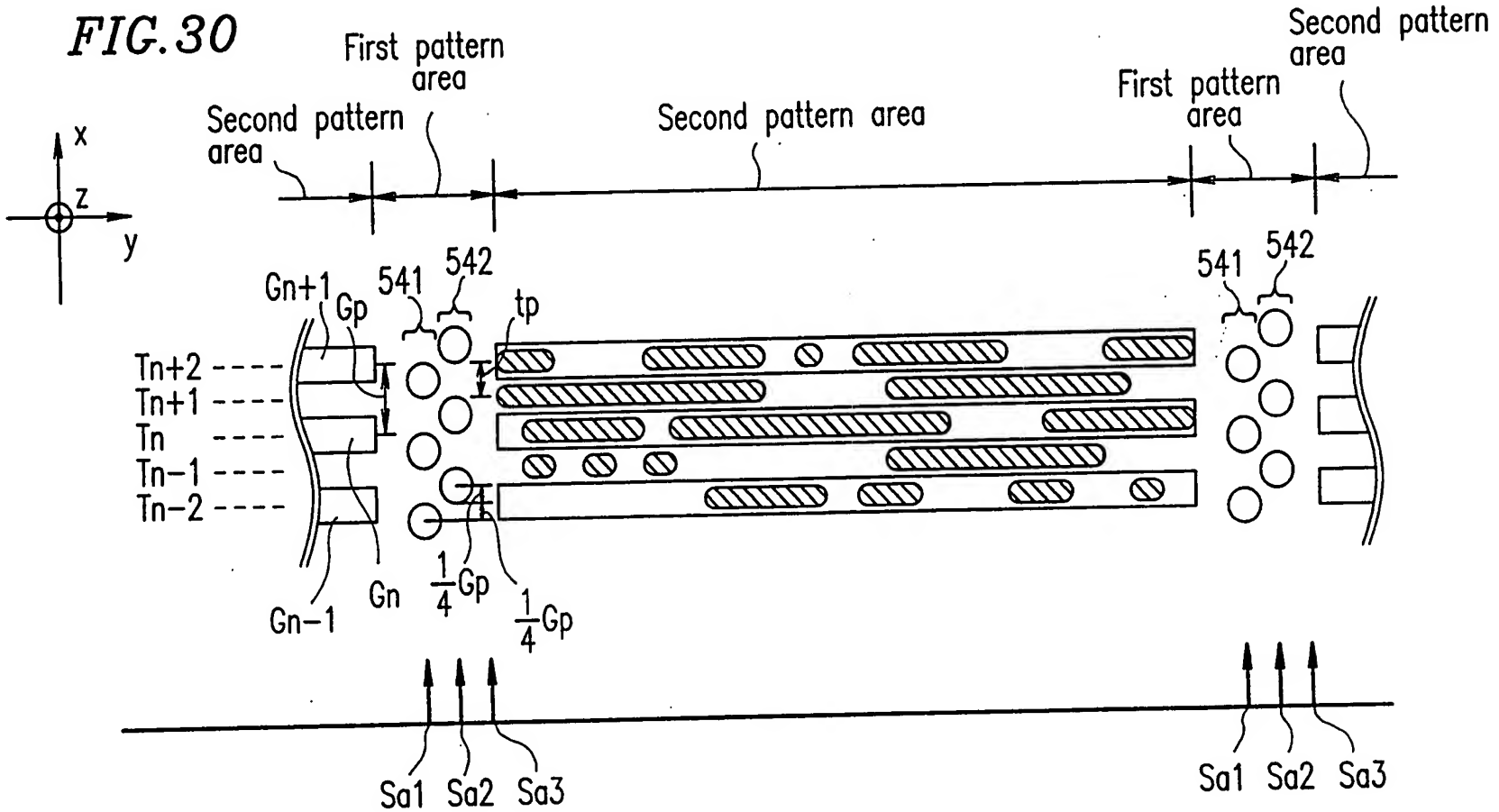

First pattern area
Second pattern area
Second pattern area
First pattern area
Second pattern area
x
z
y
Gn+1
Gp
541
542
tp
541
542
Tn+2
Tn+1
Tn
Tn-1
Tn-2
Gn-1
Gn
1/4 Gp
1/4 Gp
Sa1
Sa2
Sa3
Sa1
Sa2
Sa3

FIG. 31A

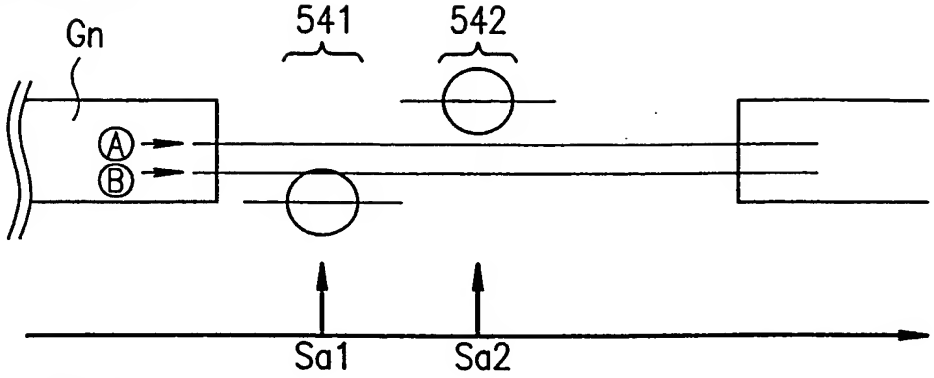


FIG. 31B

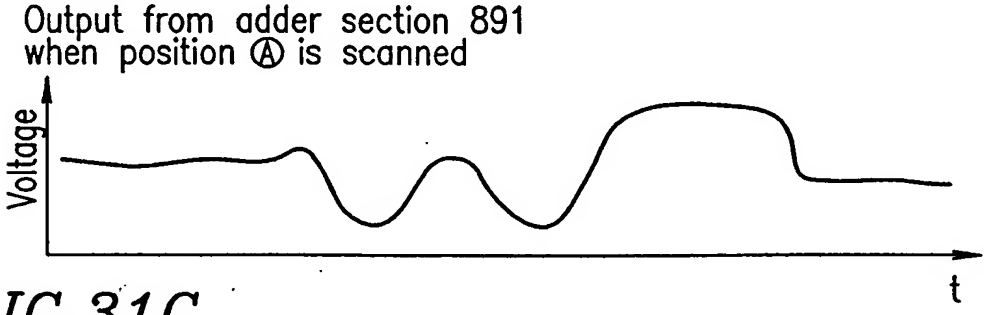


FIG. 31C

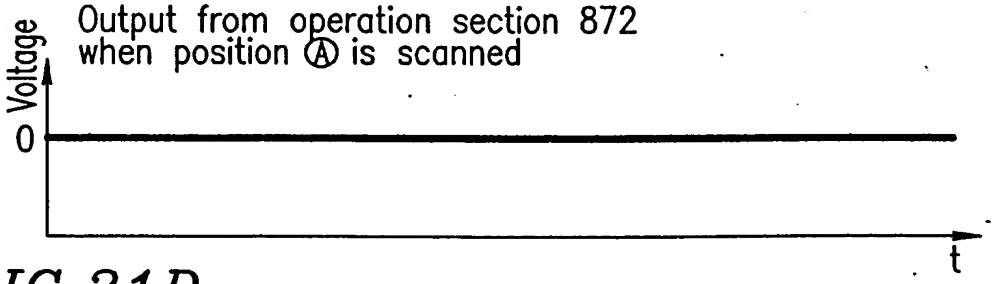


FIG. 31D

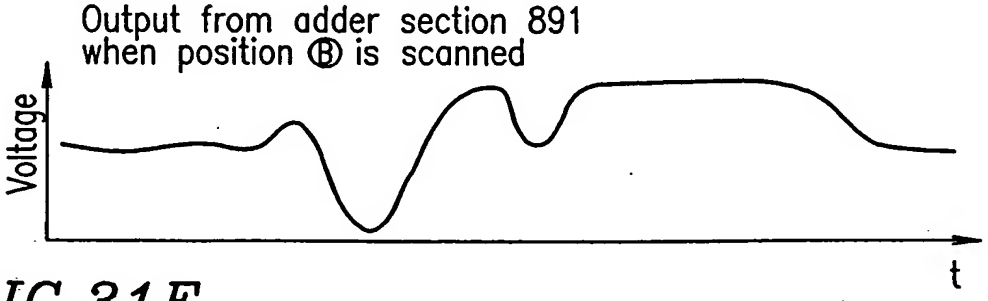


FIG. 31E

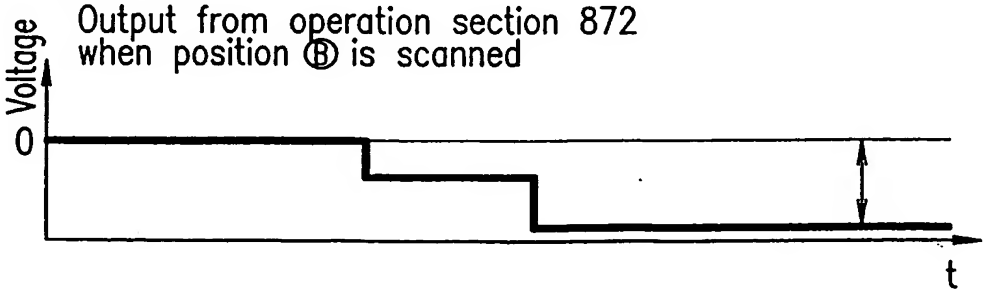
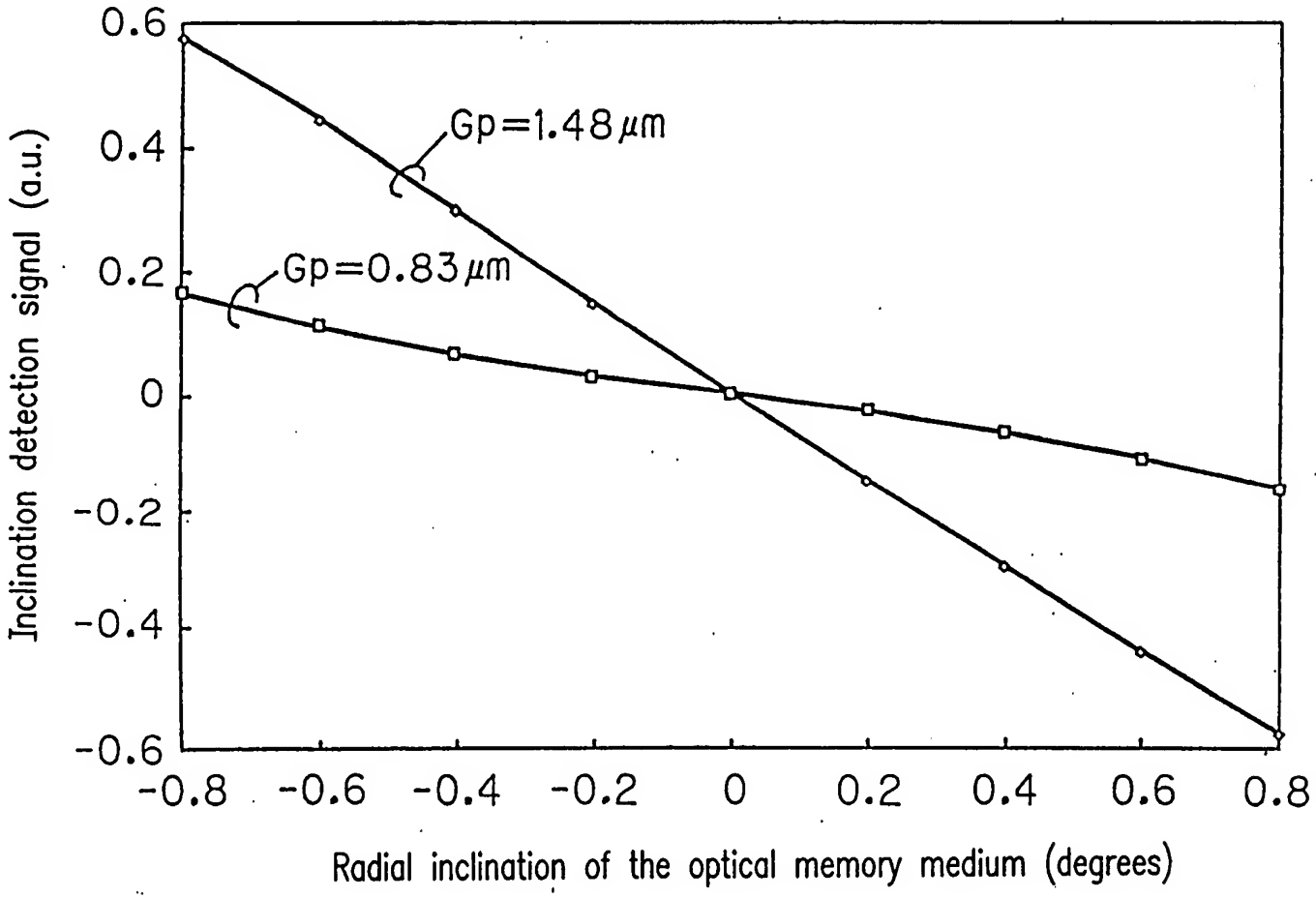


FIG.32


0.6
0.4
0.2
0
-0.2
-0.4
-0.6
Inclination detection signal (a.u.)
Gp=1.48 μm
Gp=0.83 μm
-0.8
-0.6
-0.4
-0.2
0
0.2
0.4
0.6
0.8
Radial inclination of the optical memory medium (degrees)

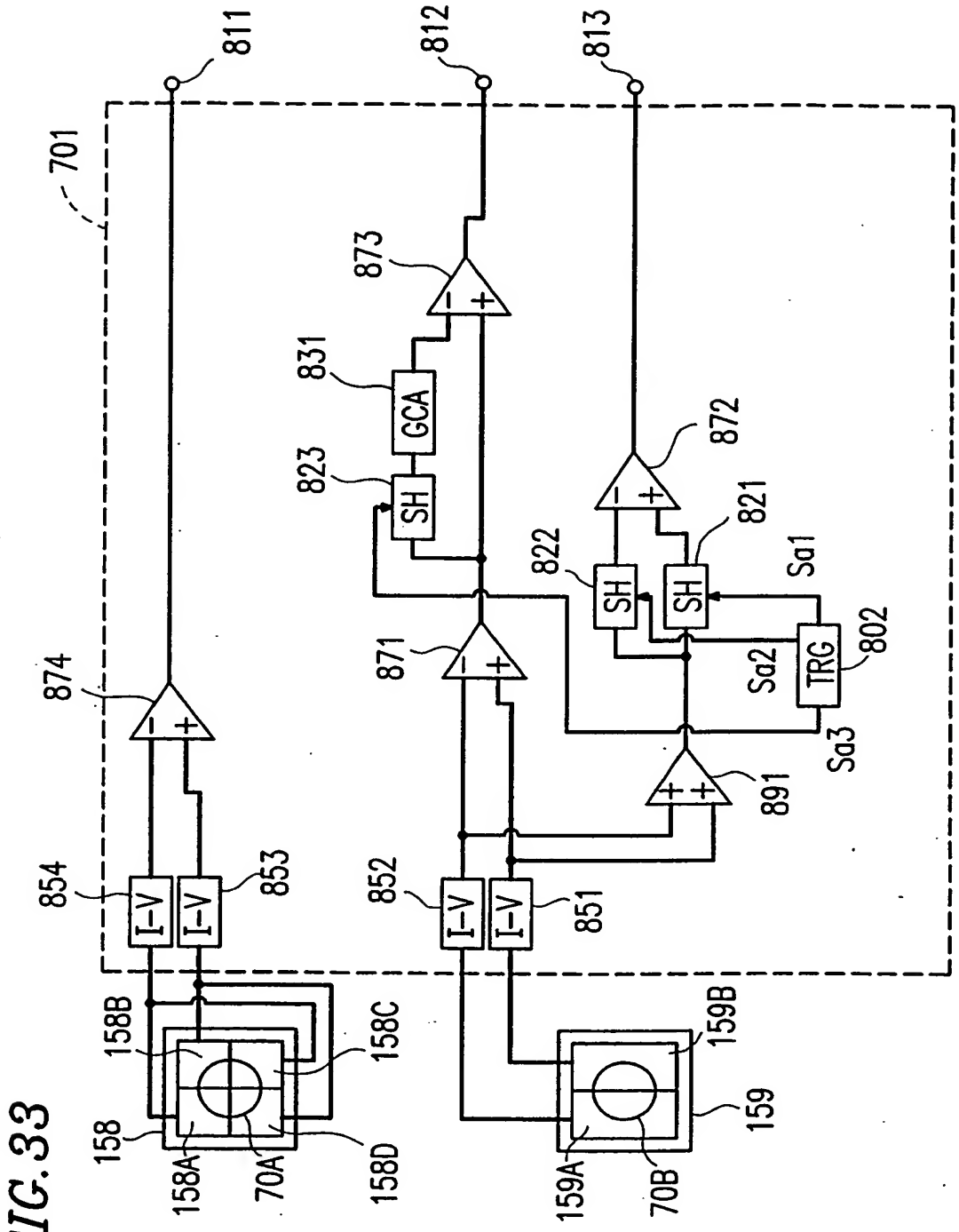
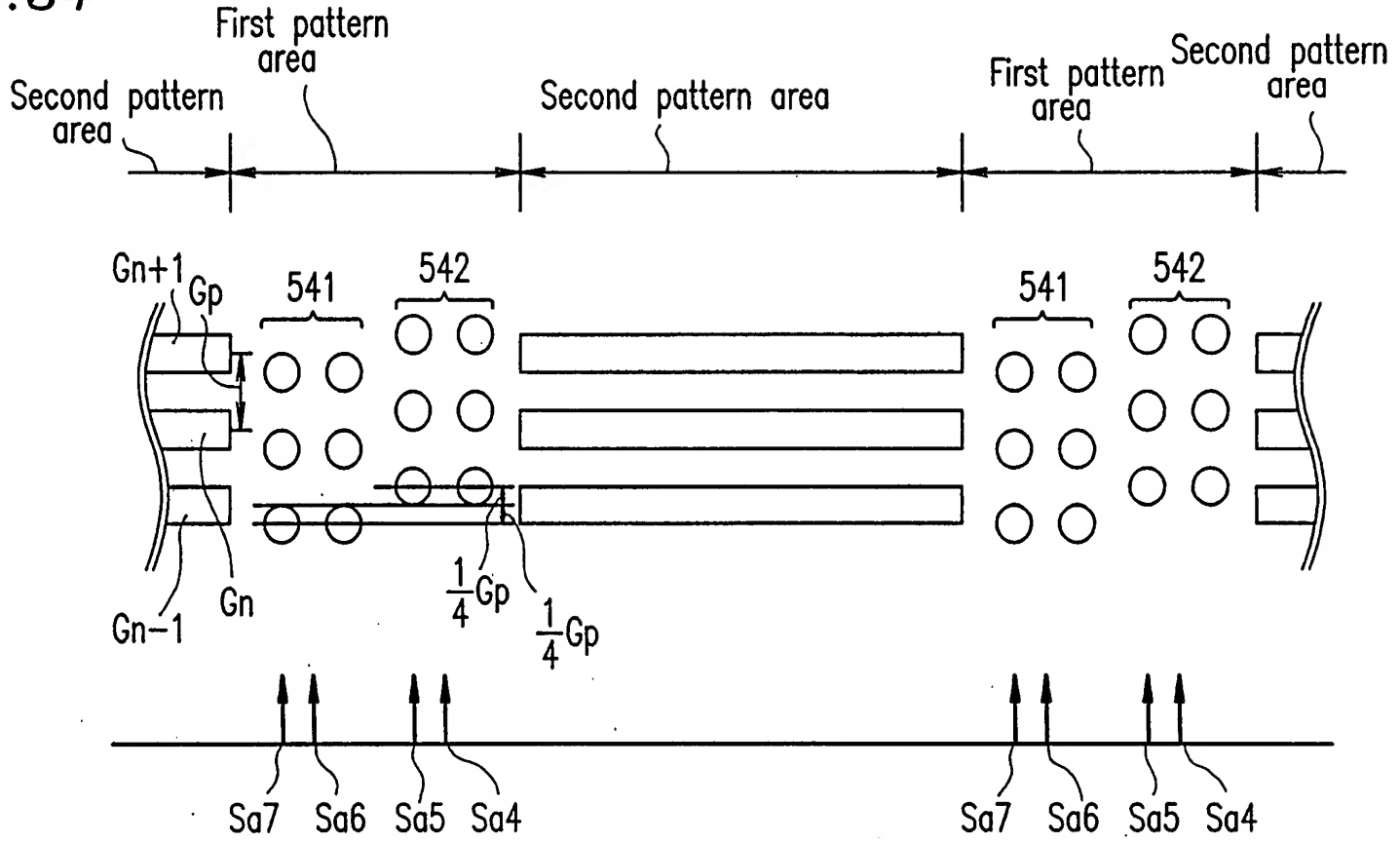

701
811
812
813
873
831
GCA
823
SH
872
821
822
SH
SH
Sa1
871
Sa2
TRG
802
874
Sa3
891
854
I-V
I-V
853
852
I-V
I-V
851
158B
158C
158
158A
70A
158D
159B
159
159A
70B

FIG. 33

FIG. 34


First pattern area
Second pattern area
Second pattern area
First pattern area
Second pattern area
Gn+1
Gp
541
542
541
542
Gn-1
Gn
1/4 Gp
1/4 Gp
Sa7
Sa6
Sa5
Sa4
Sa7
Sa6
Sa5
Sa4

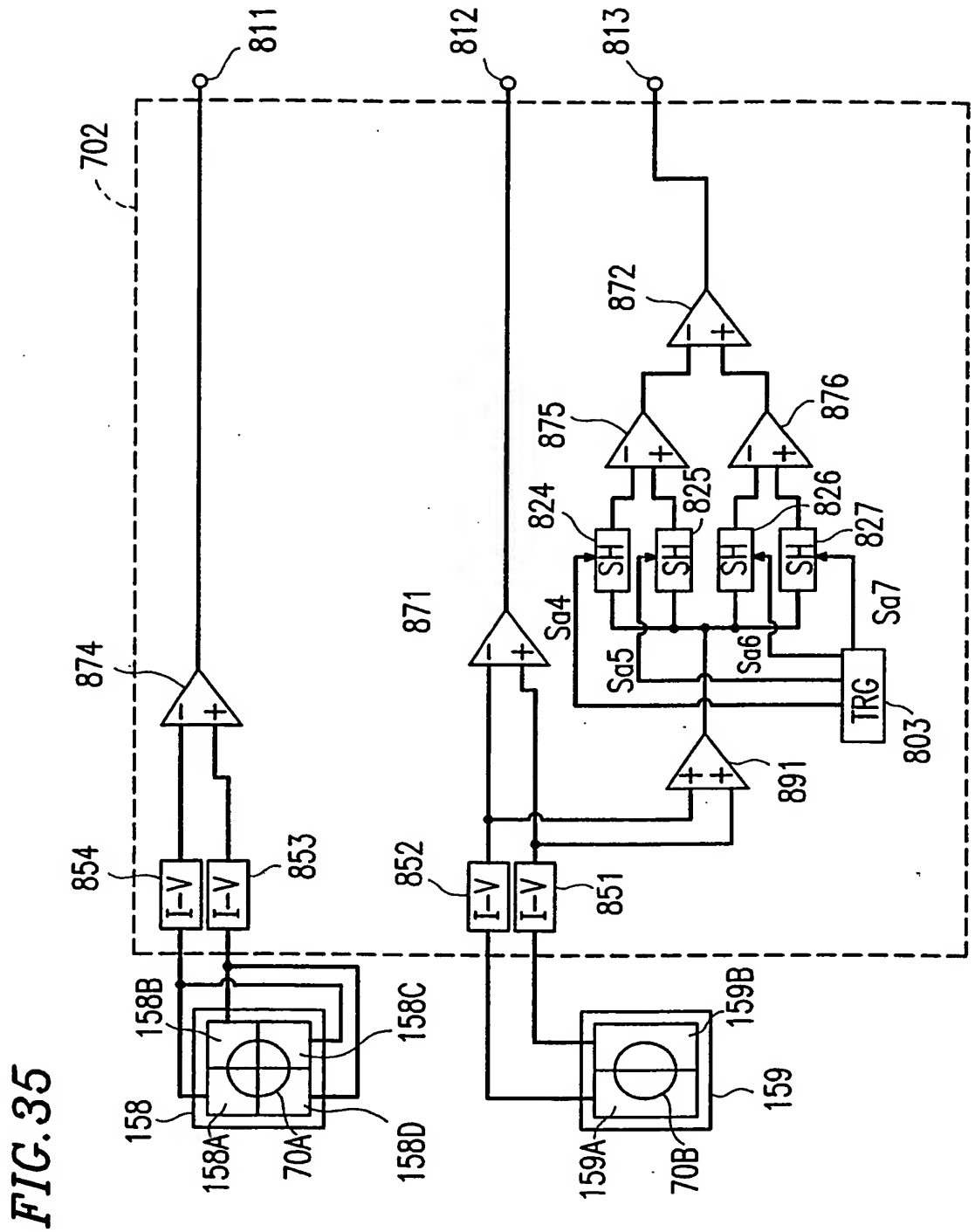

702
811
812
813
872
875
876
824
825
826
827
SH
Sa4
Sa5
Sa6
Sa7
871
874
TRG
803
891
854
853
852
851
I-V
158B
158C
158
158A
70A
158D
159B
159
159A
70B

FIG. 35

FIG. 36

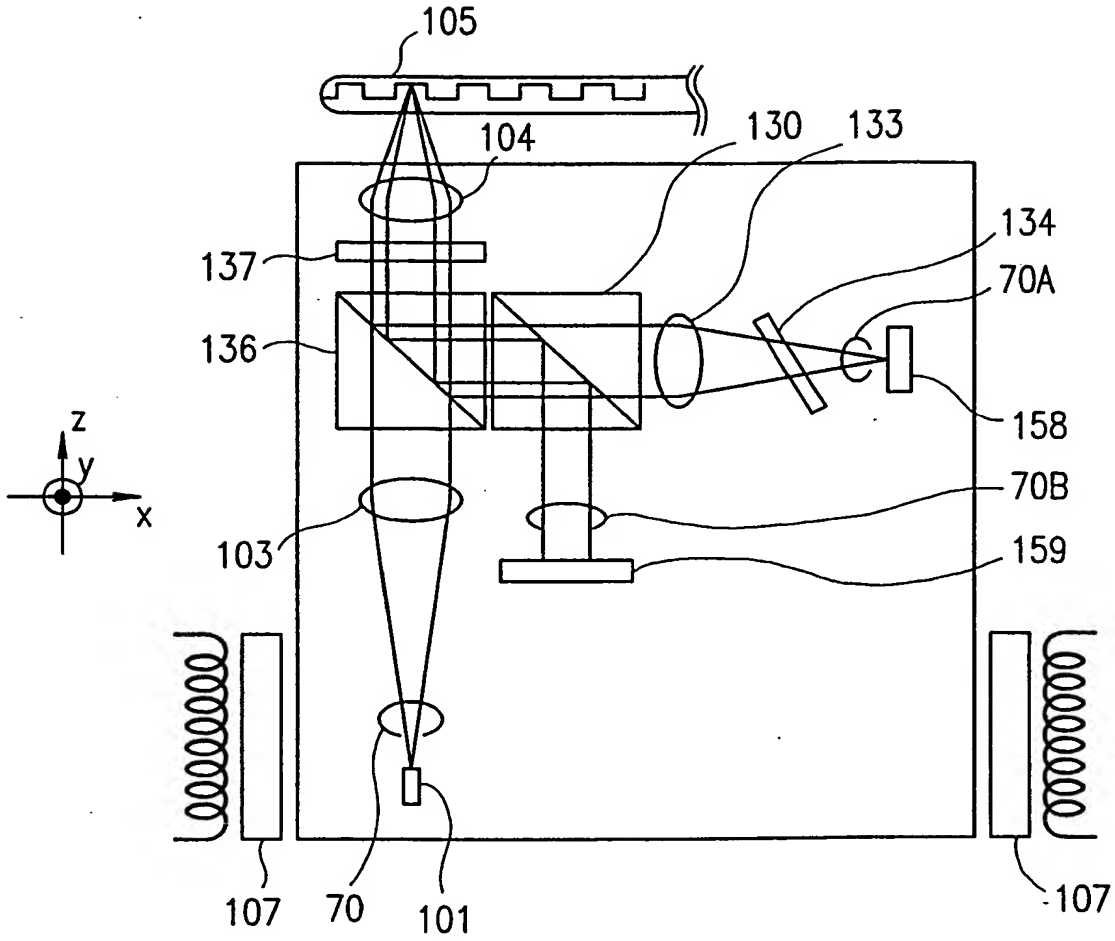

105
104
130
133
134
137
70A
136
158
z
y
x
70B
103
159
107
70
101
107

FIG. 37

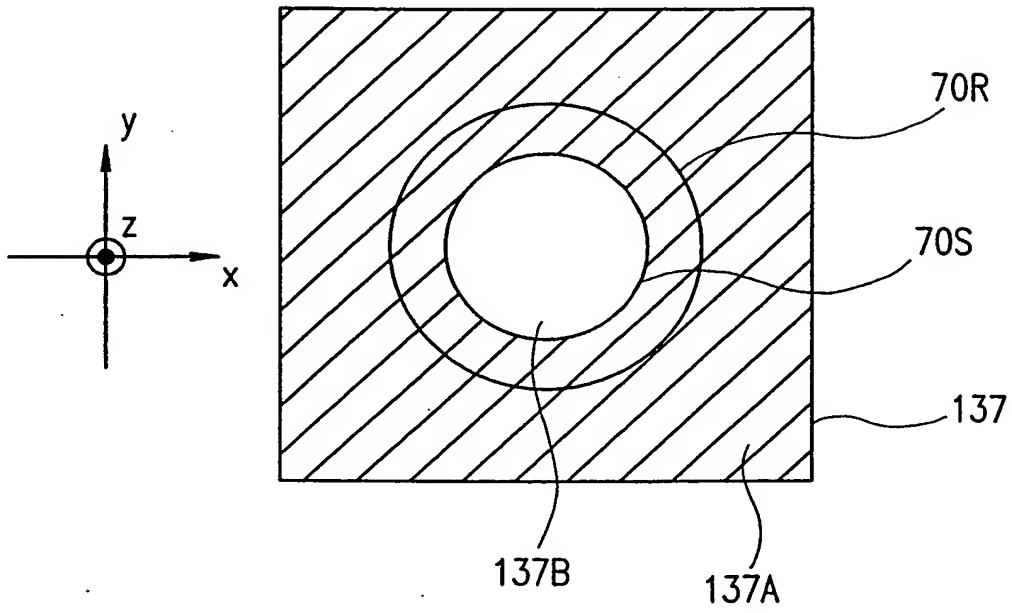


FIG. 38

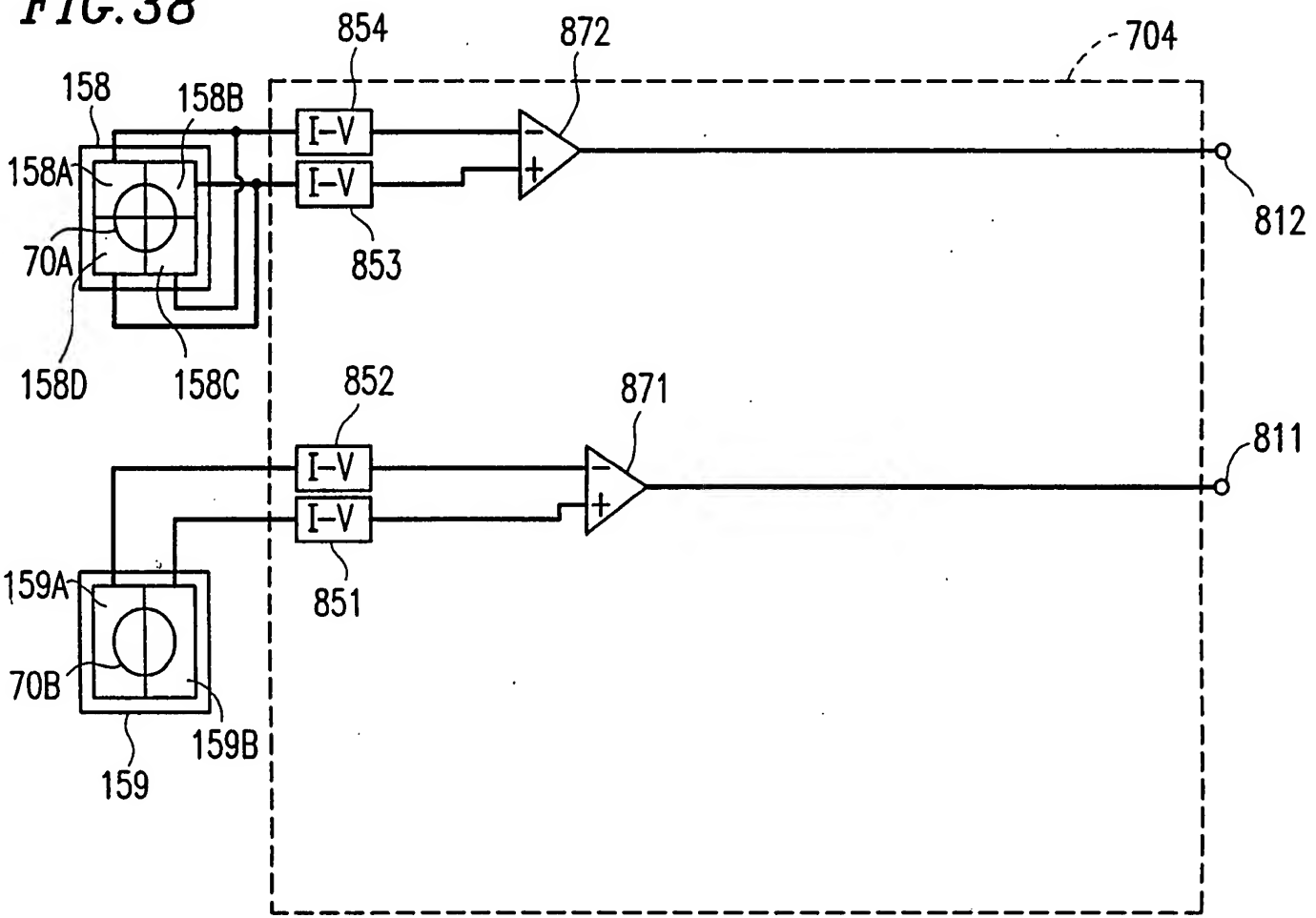

854
872
704
158
158B
158A
I-V
I-V
812
70A
853
158D
158C
852
871
811
I-V
I-V
159A
851
70B
159B
159

FIG. 39

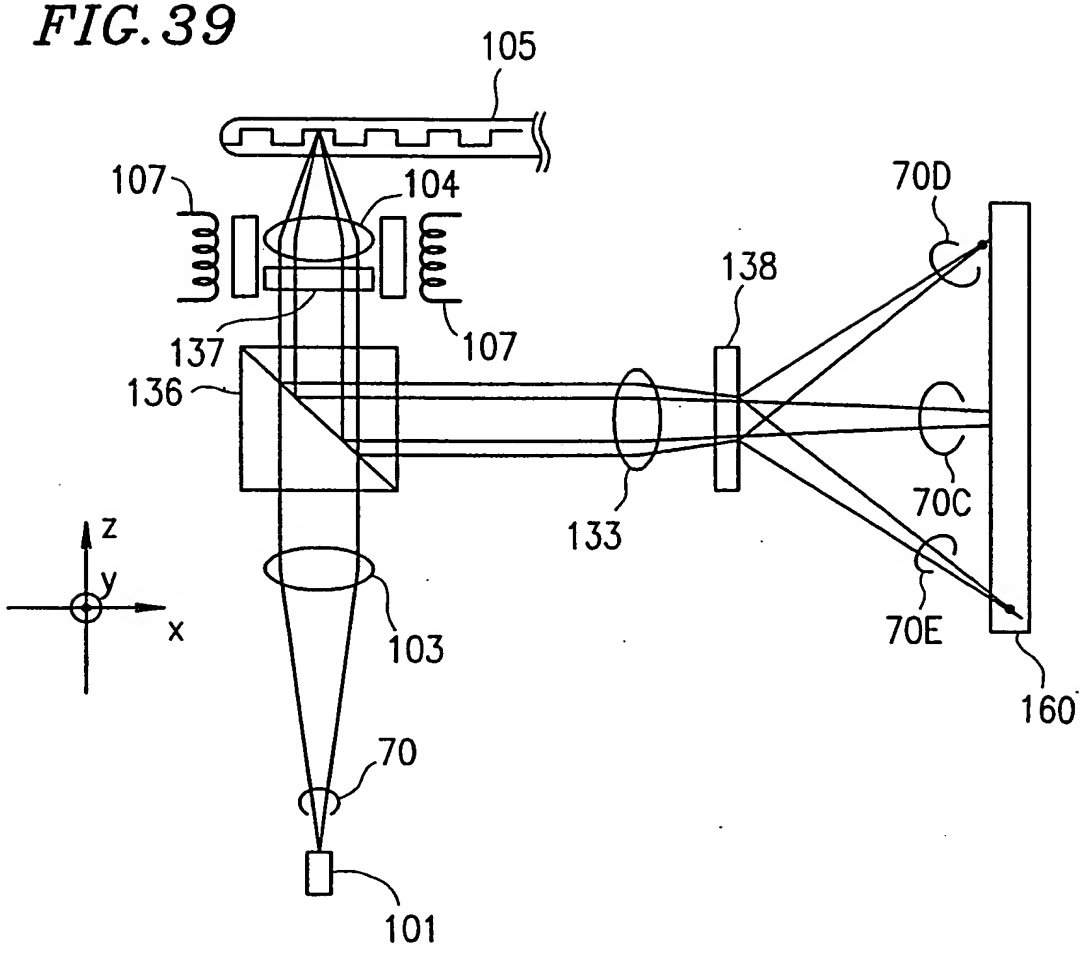


FIG. 40

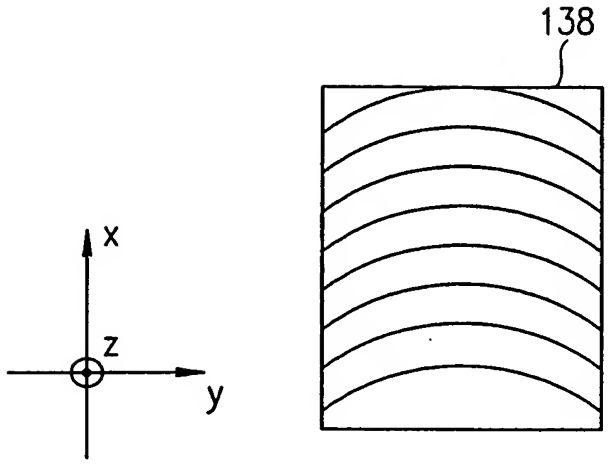


FIG. 41

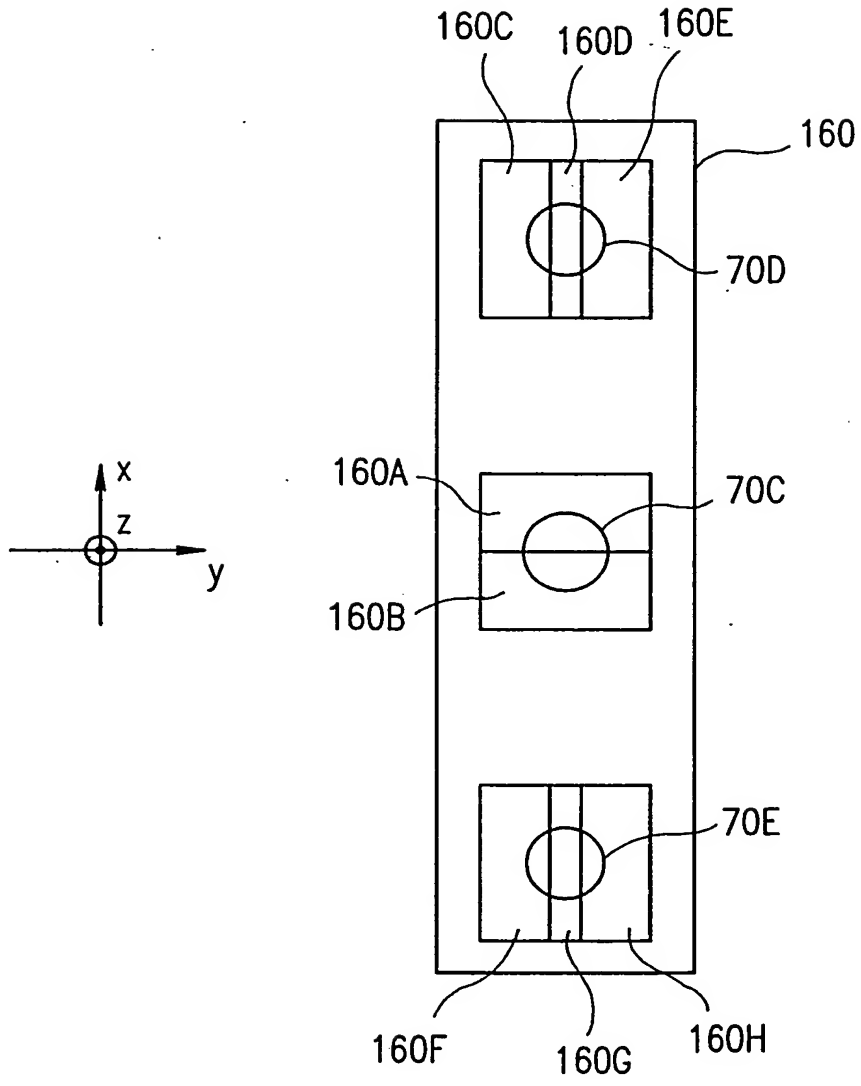


FIG. 42

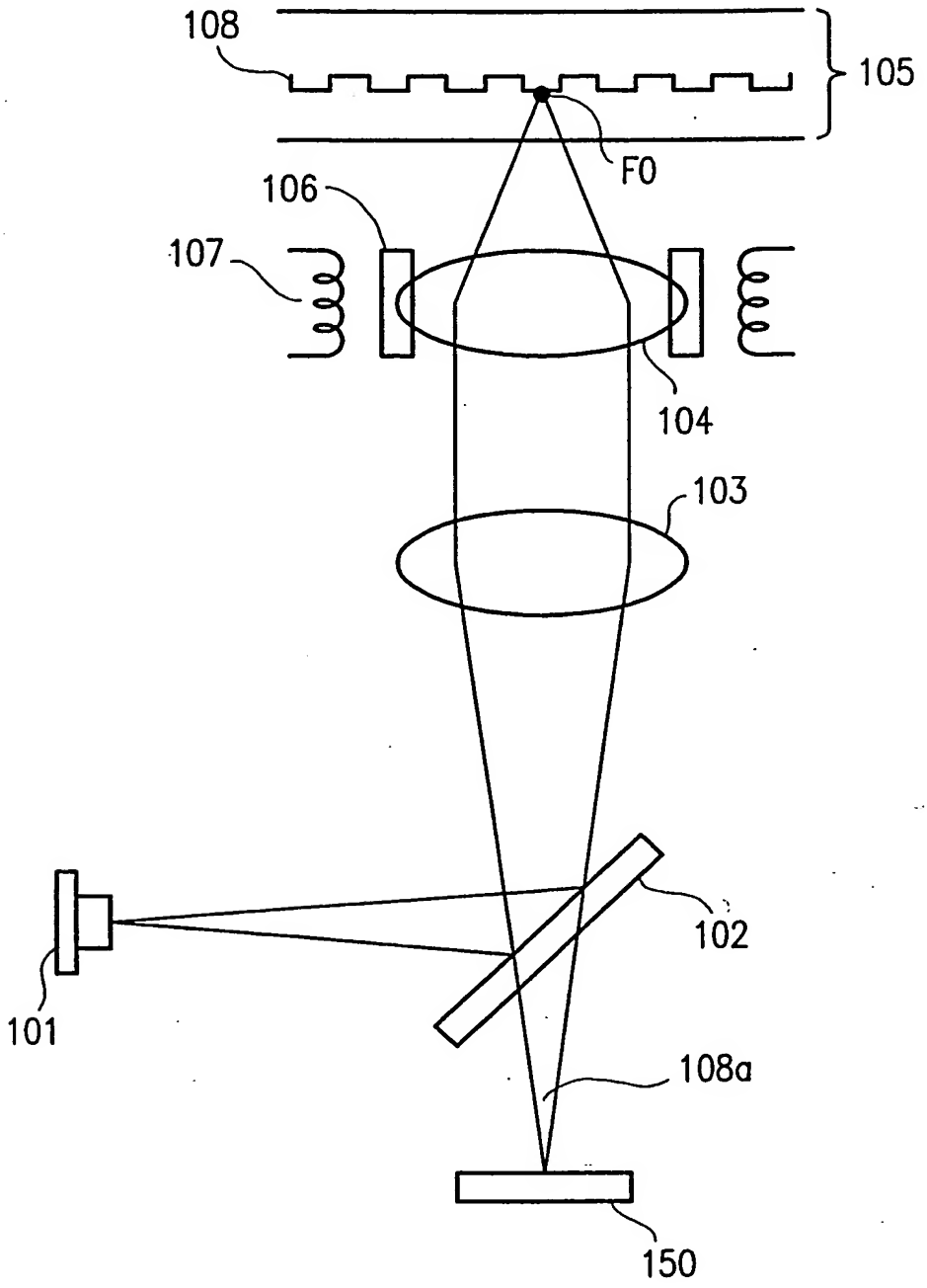


FIG. 43A

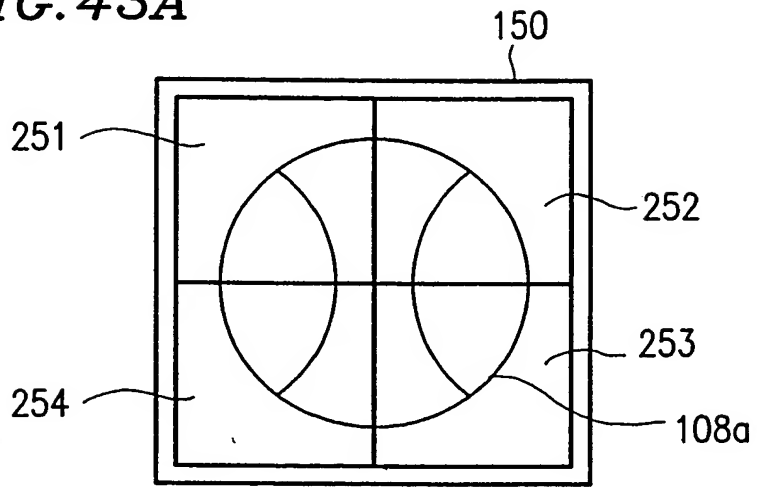


FIG. 43B

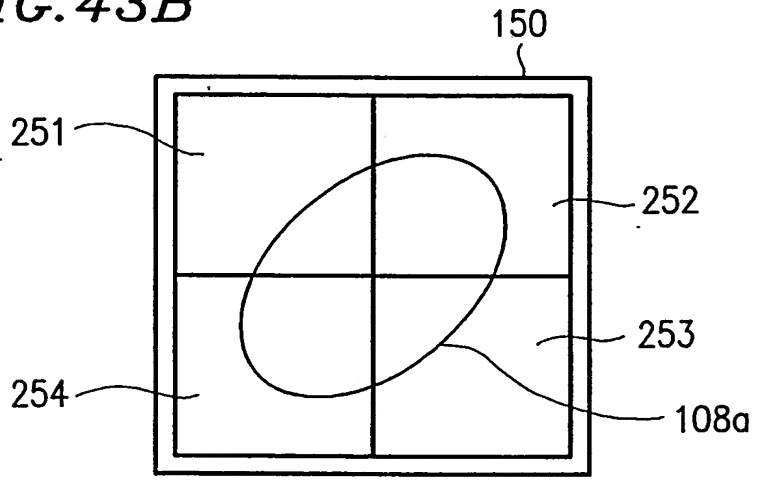


FIG. 43C

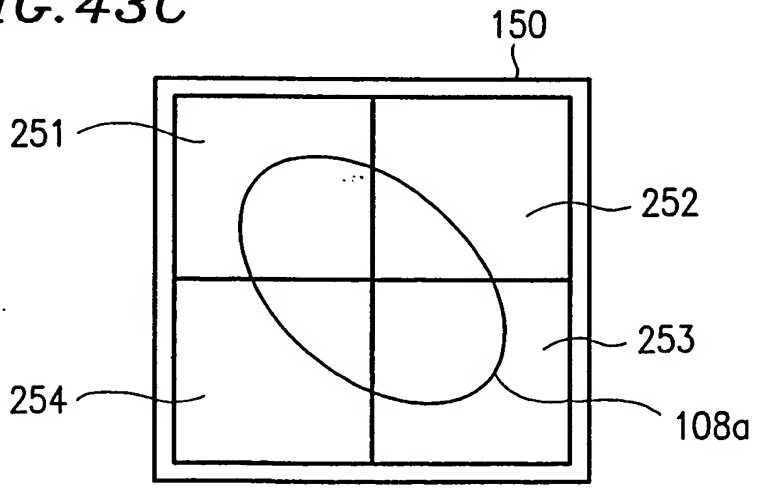


FIG. 44

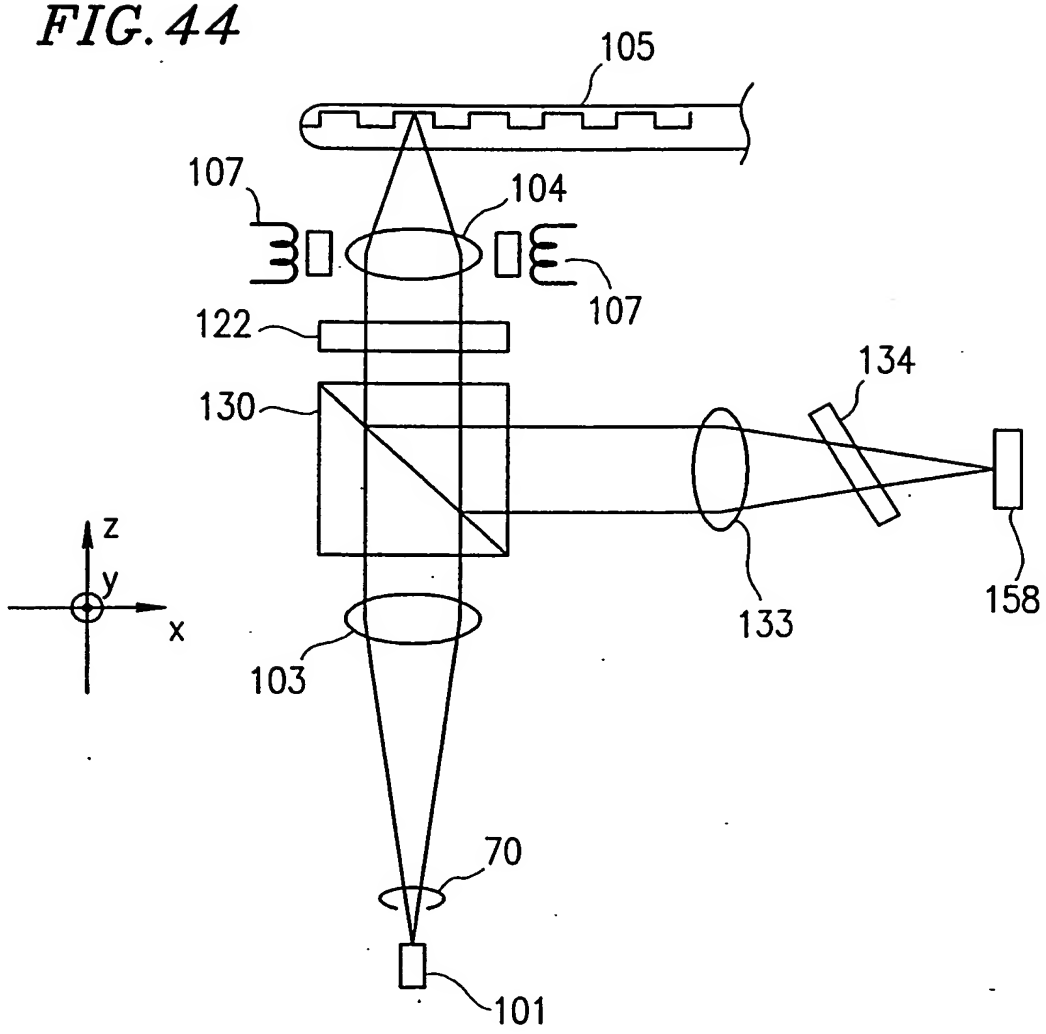


FIG. 45

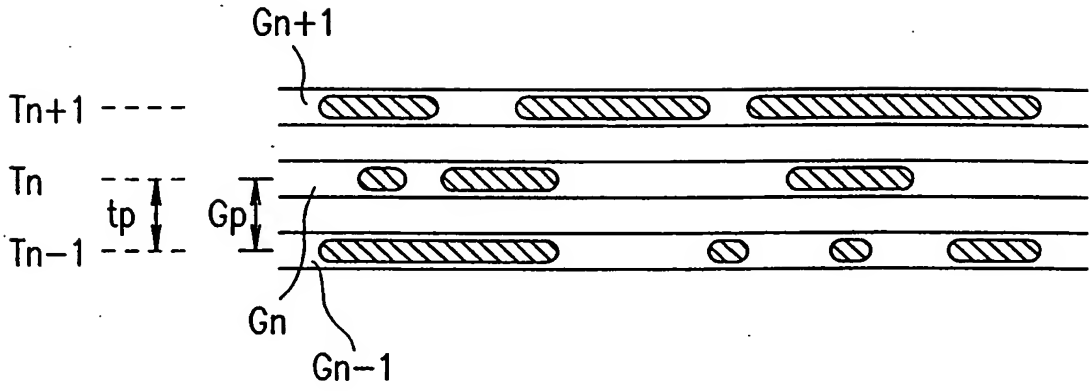


FIG. 46

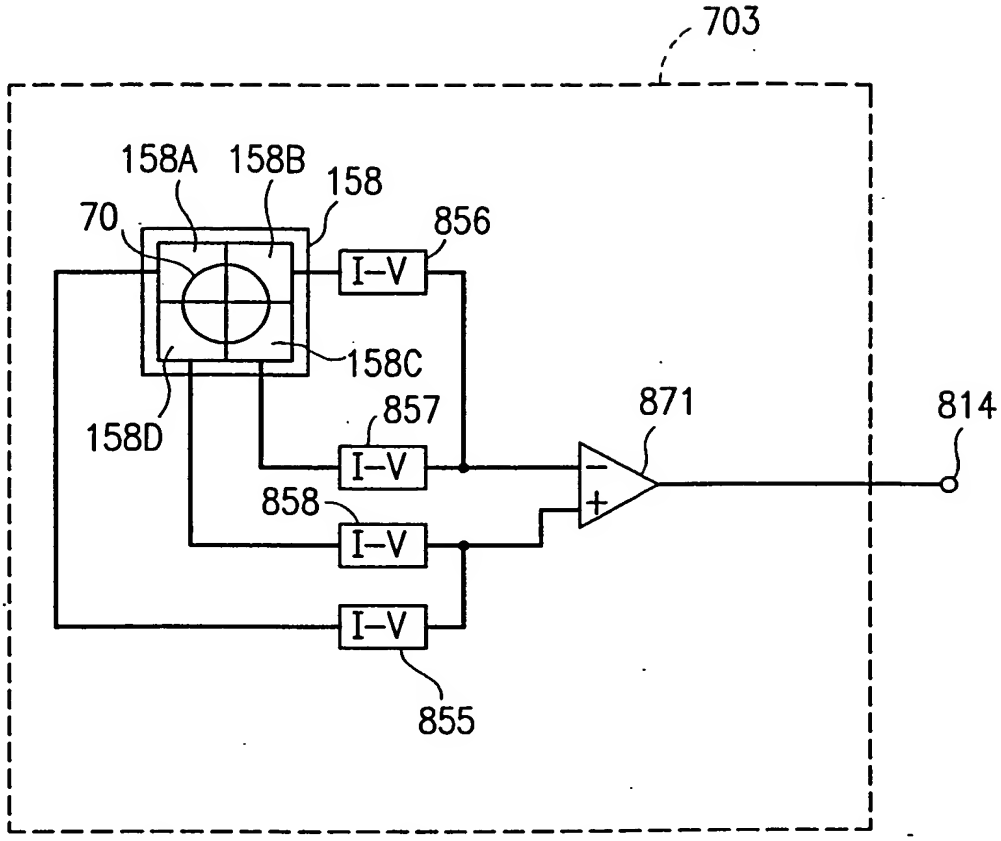
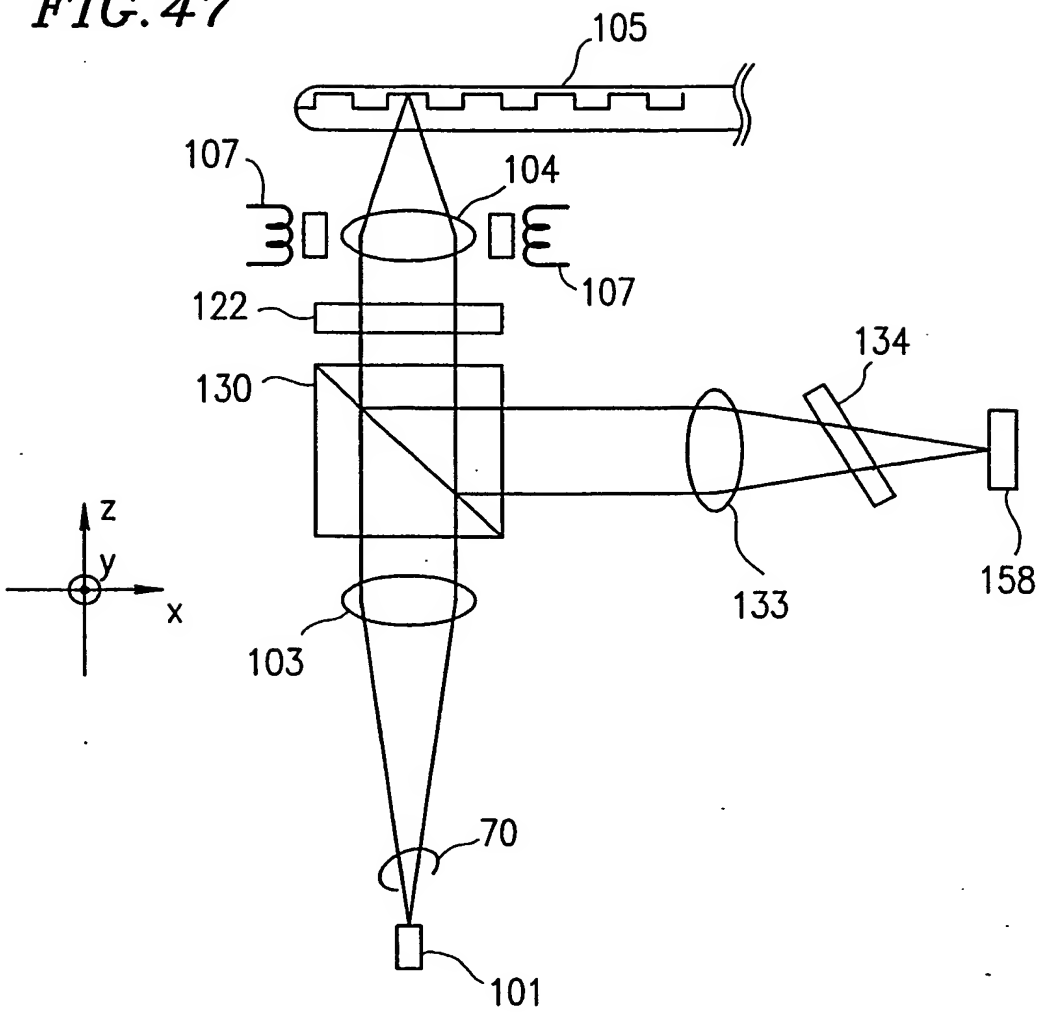


FIG. 47



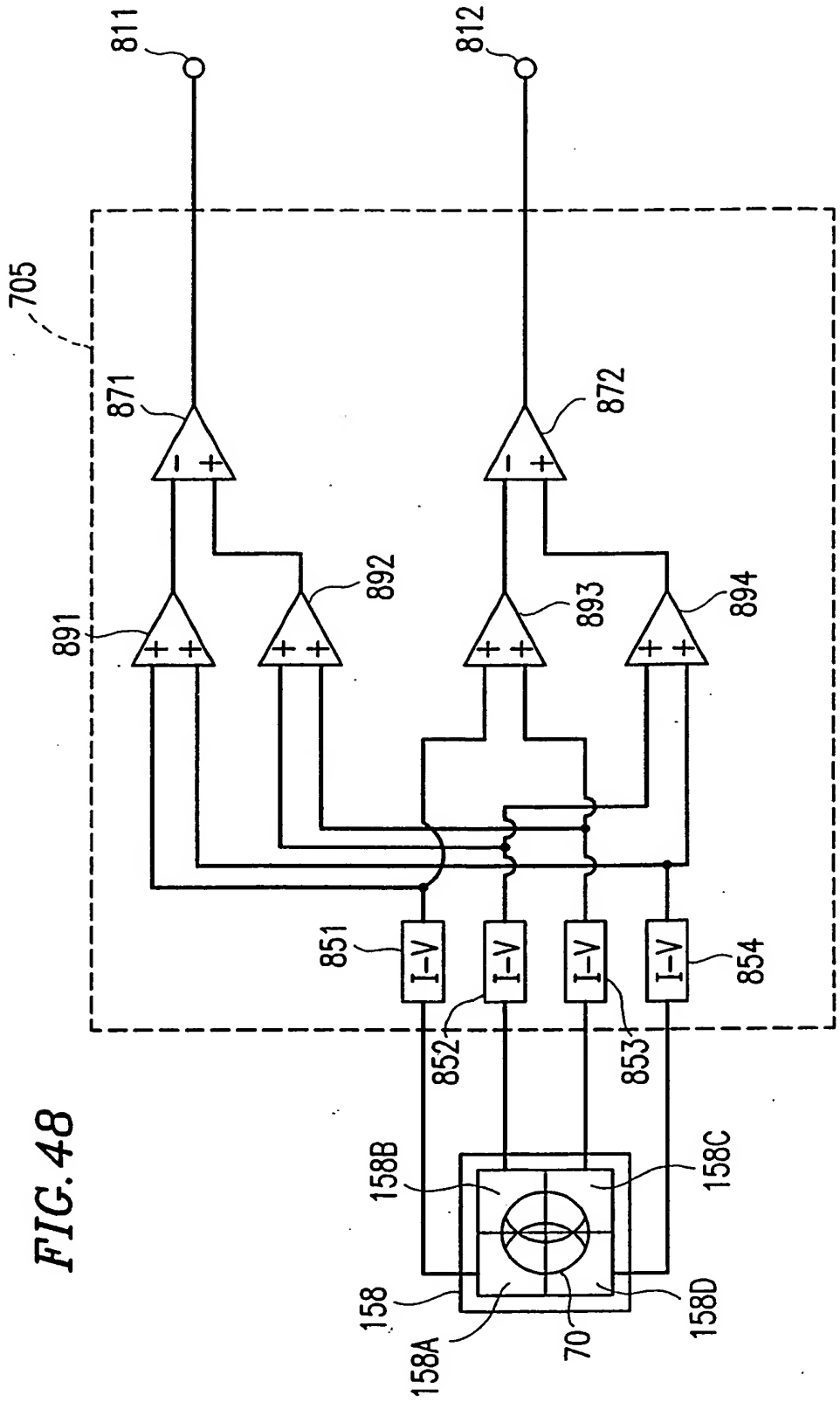

811
812
705
871
872
891
892
893
894
851
I-V
852
853
854
158B
158C
158
158A
70
158D

FIG. 48

FIG. 49

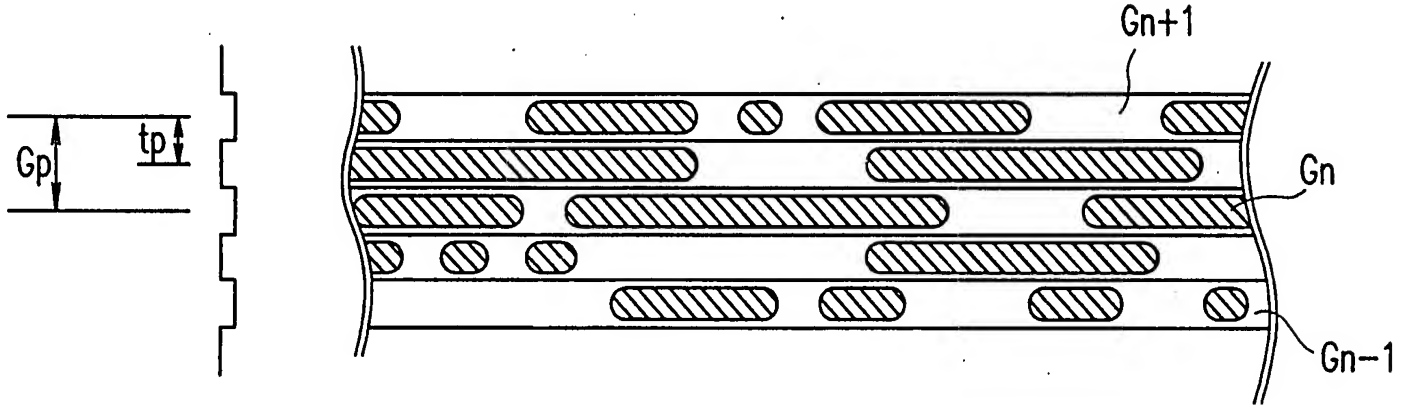


FIG. 50

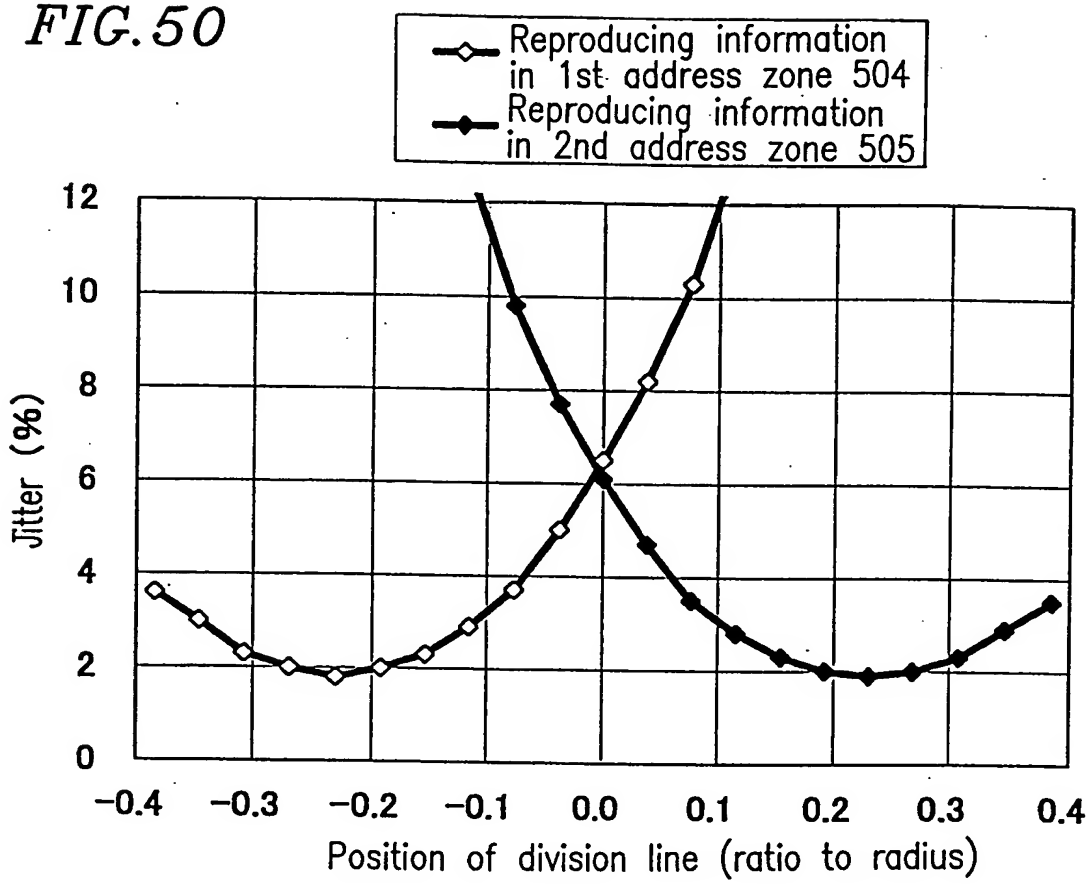

Reproducing information in 1st address zone 504
Reproducing information in 2nd address zone 505
Jitter (%)
12
10
8
6
4
2
0
−0.4
−0.3
−0.2
−0.1
0.0
0.1
0.2
0.3
0.4
Position of division line (ratio to radius)

FIG. 51

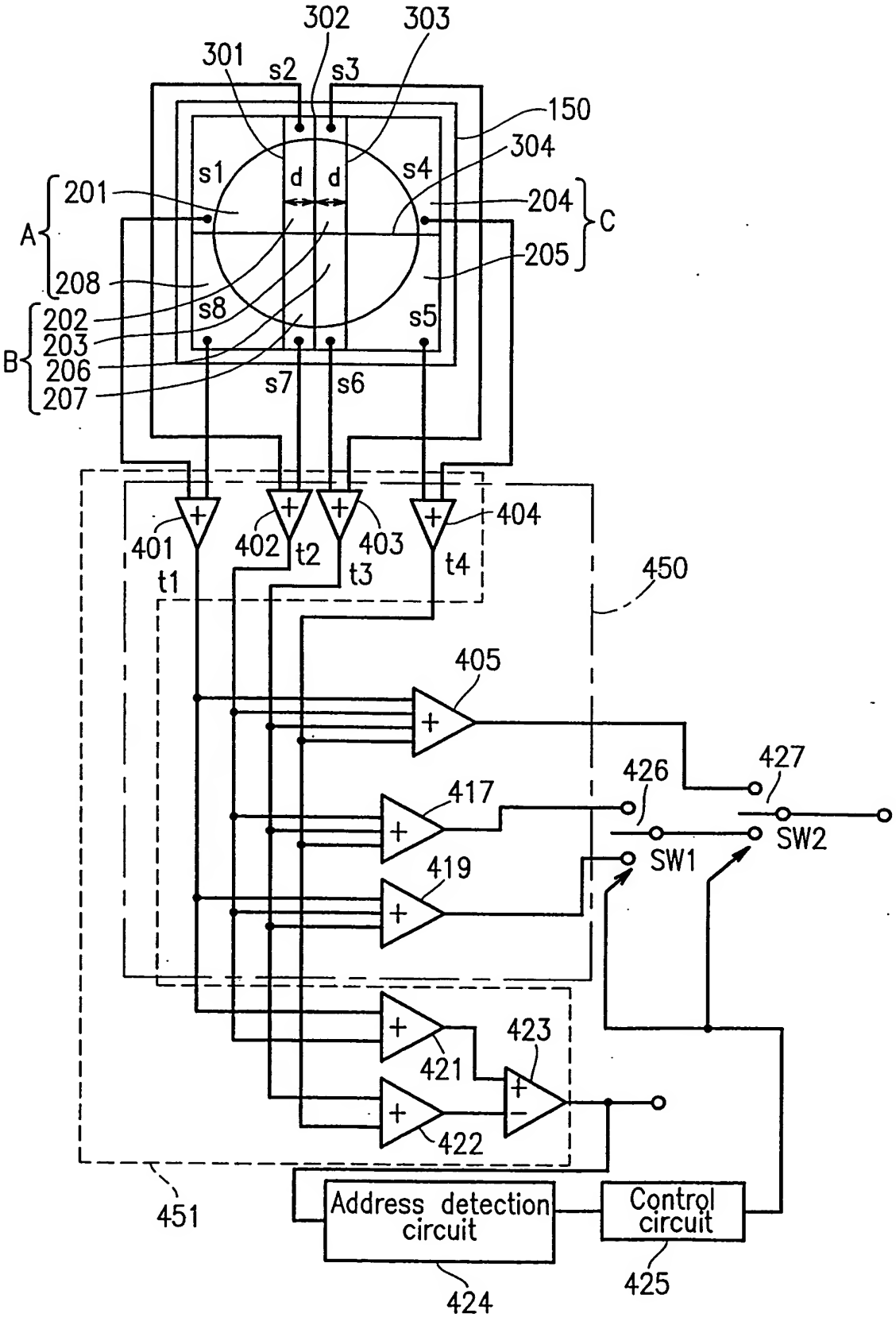

302
303
301
s2
s3
150
304
s1
d
d
s4
201
204
C
A
205
208
s8
s5
202
203
206
207
B
s7
s6
401
402
403
404
t1
t2
t3
t4
450
405
427
426
417
SW1
SW2
419
423
421
422
451
Address detection circuit
Control circuit
424
425

FIG. 52A

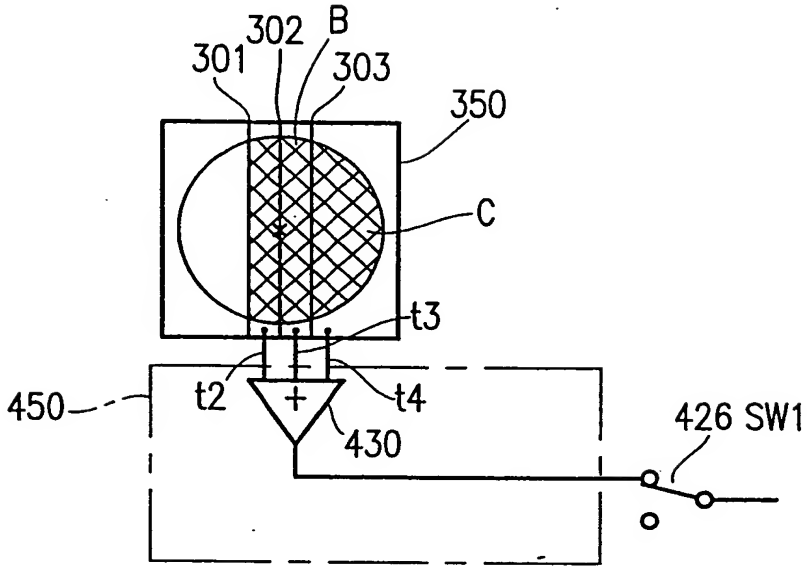


FIG. 52B

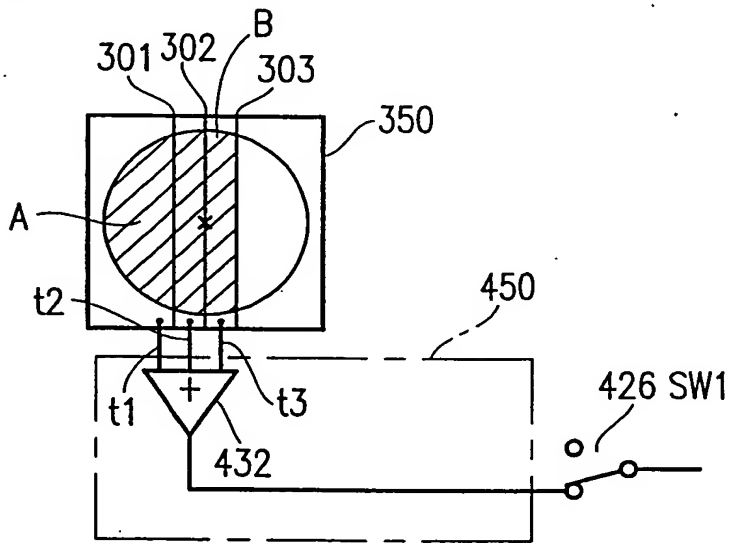


FIG. 53

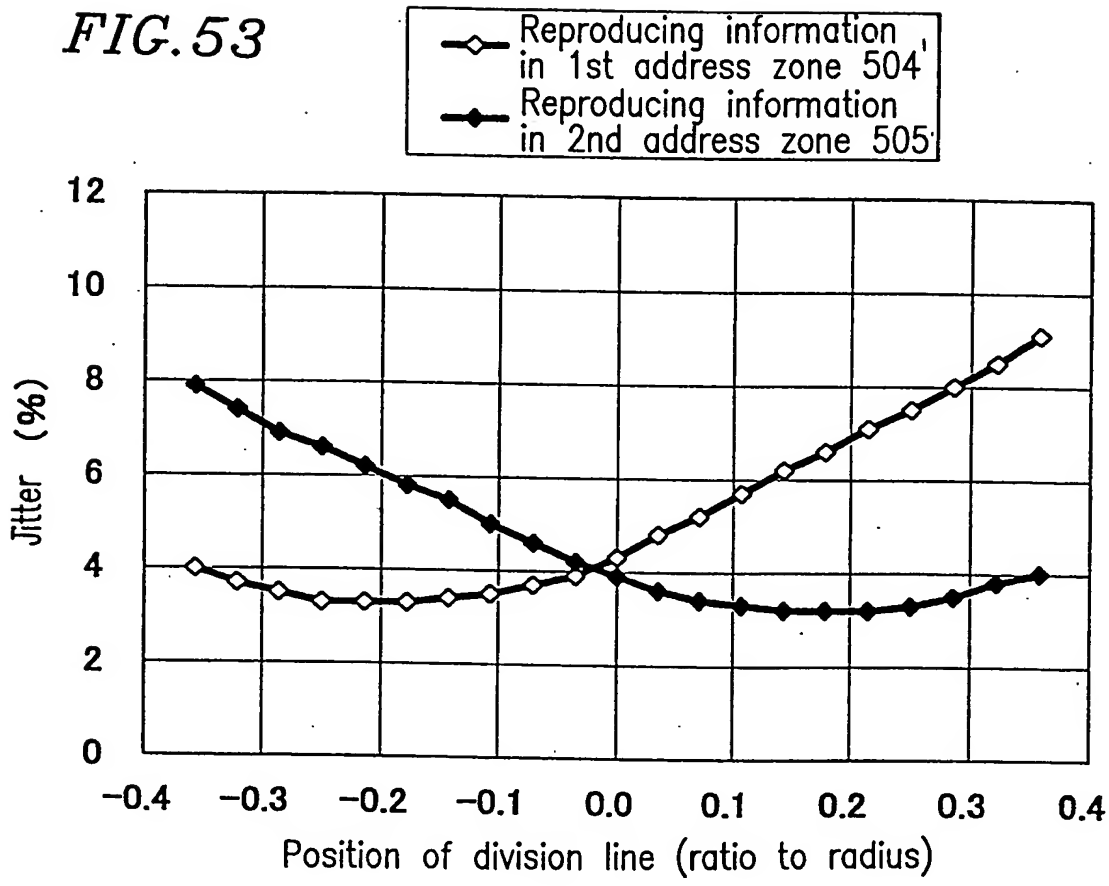

Reproducing information in 1st address zone 504
Reproducing information in 2nd address zone 505
Jitter (%)
12
10
8
6
4
2
0
−0.4
−0.3
−0.2
−0.1
0.0
0.1
0.2
0.3
0.4
Position of division line (ratio to radius)

FIG. 54

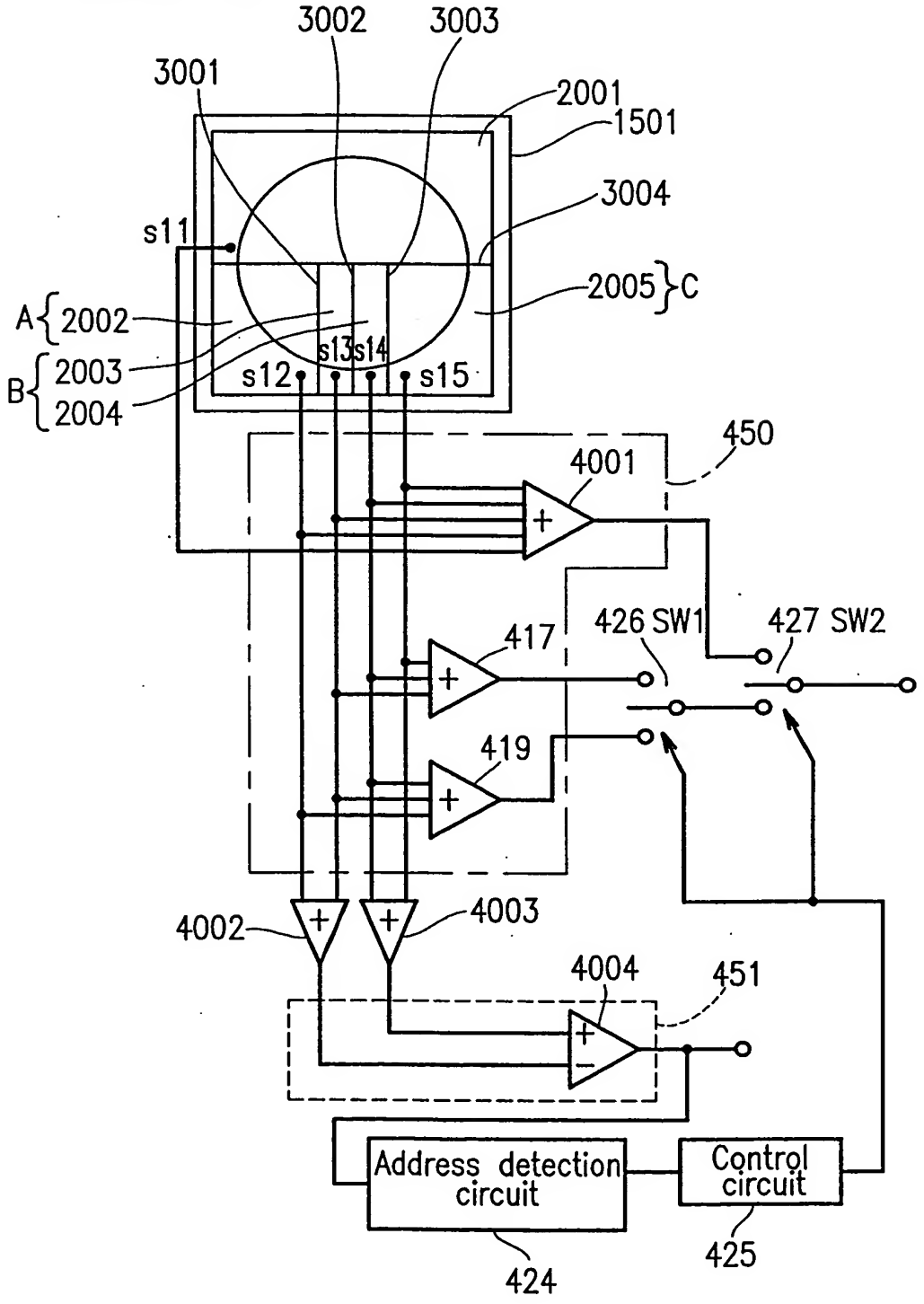

3002
3003
3001
2001
1501
3004
s11
2005
C
A
2002
2003
B
2004
s12
s13
s14
s15
450
4001
417
426 SW1
427 SW2
419
4002
4003
4004
451
Address detection circuit
Control circuit
424
425

FIG. 55

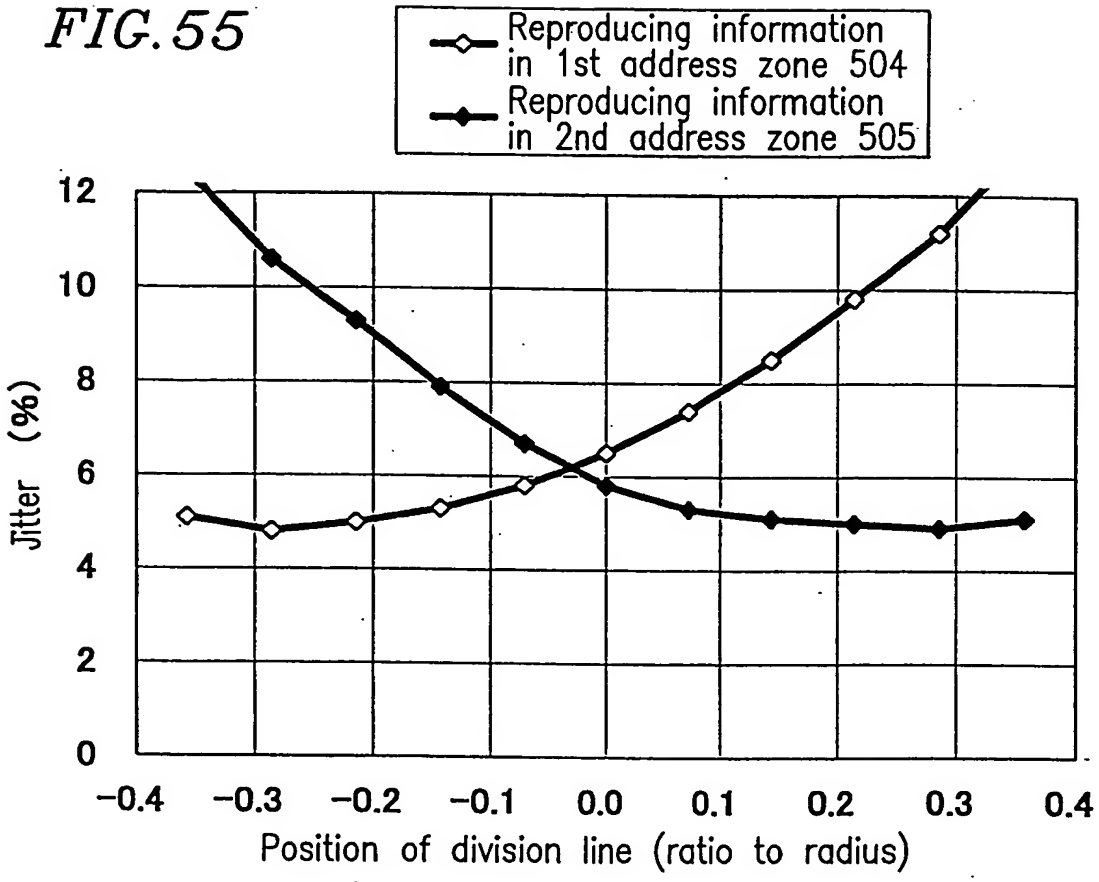

Reproducing information in 1st address zone 504
Reproducing information in 2nd address zone 505
Jitter (%)
12
10
8
6
4
2
0
−0.4
−0.3
−0.2
−0.1
0.0
0.1
0.2
0.3
0.4
Position of division line (ratio to radius)

FIG. 56A

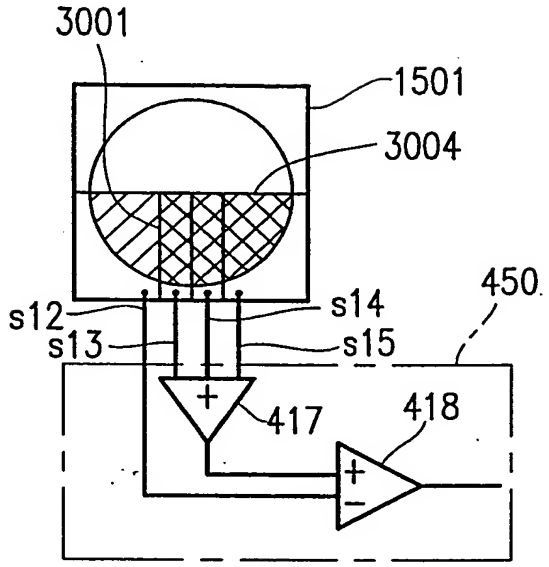


FIG. 56B

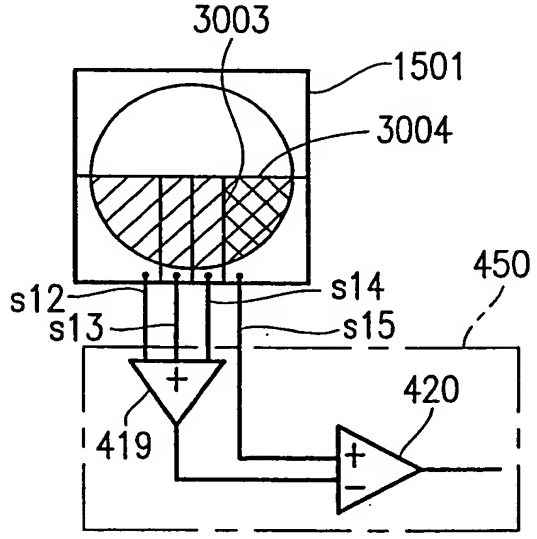


FIG. 57A

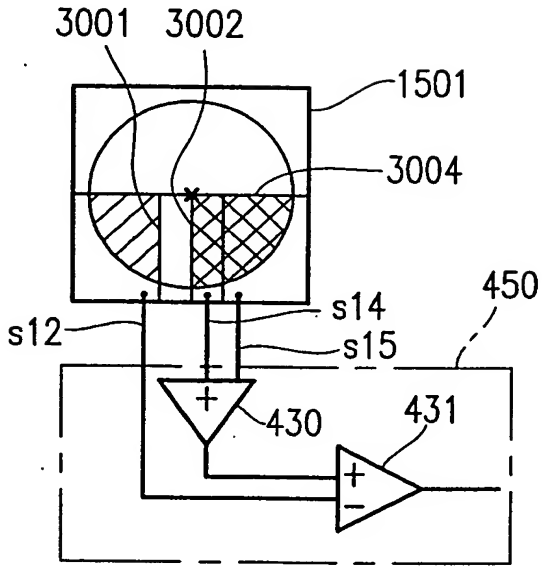


FIG. 57B

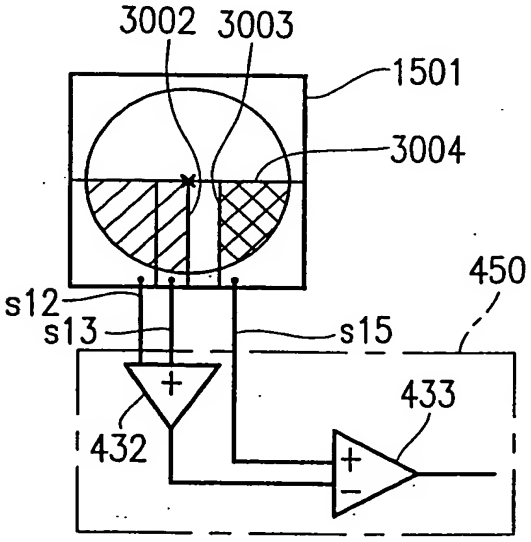


FIG. 58

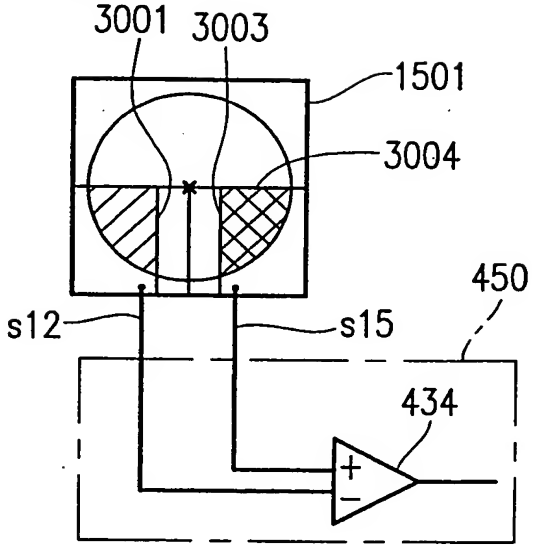
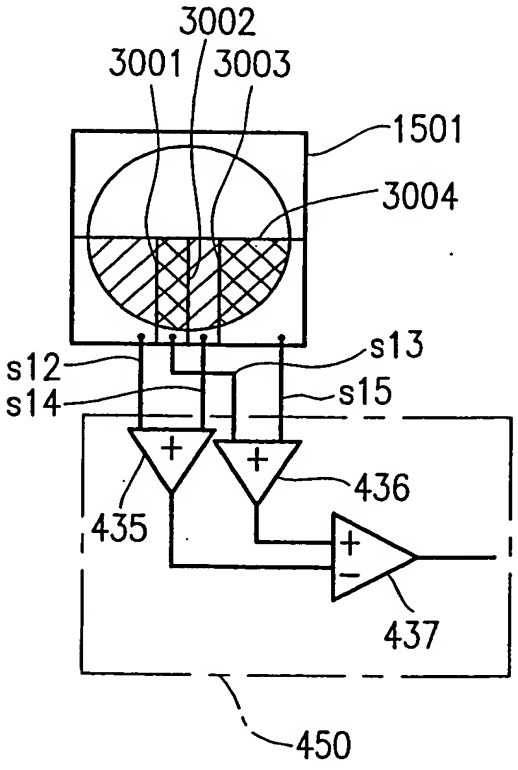

3001
3003
1501
3004
450
s12
s15
434
+
−

FIG. 59


3002
3001
3003
1501
3004
s13
s12
s14
s15
+
+
436
435
+
−
437
450